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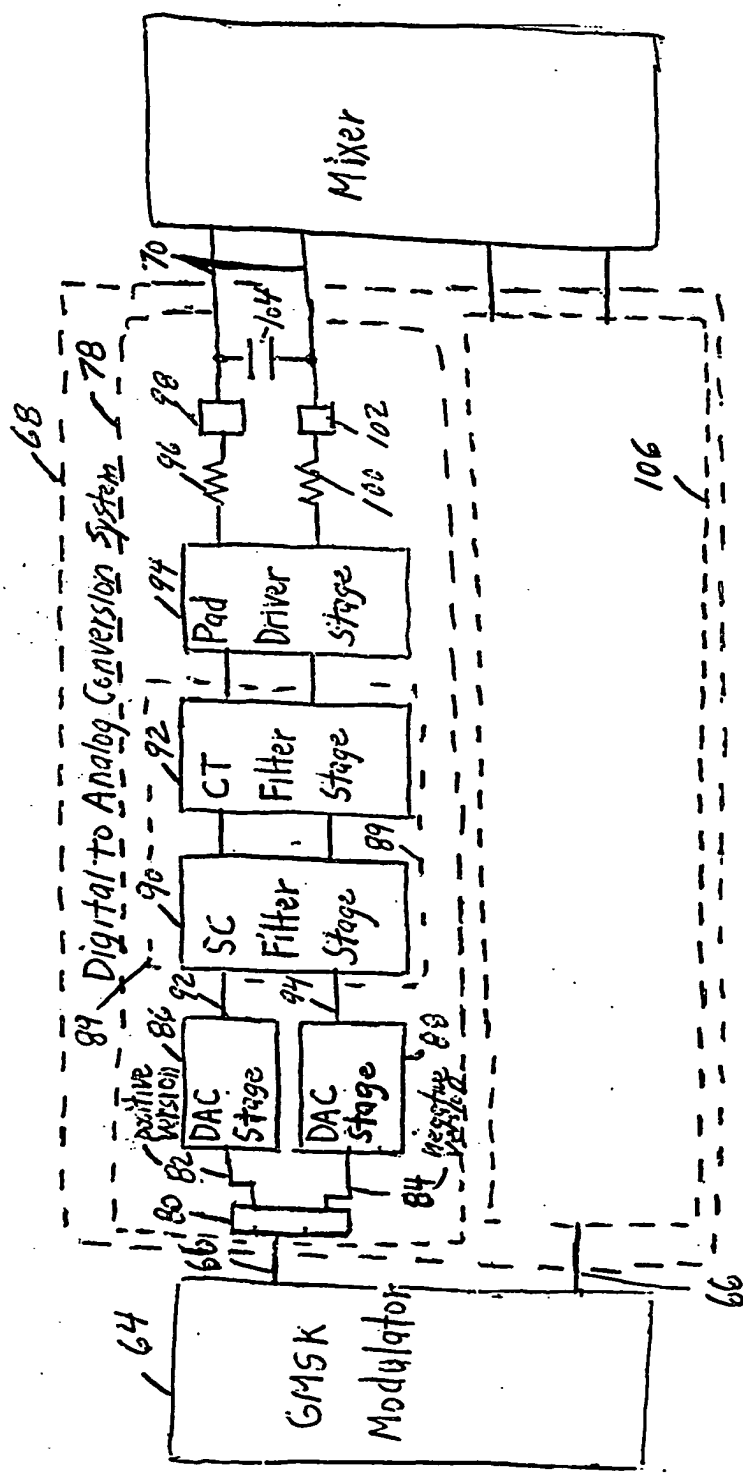


FIG. 2

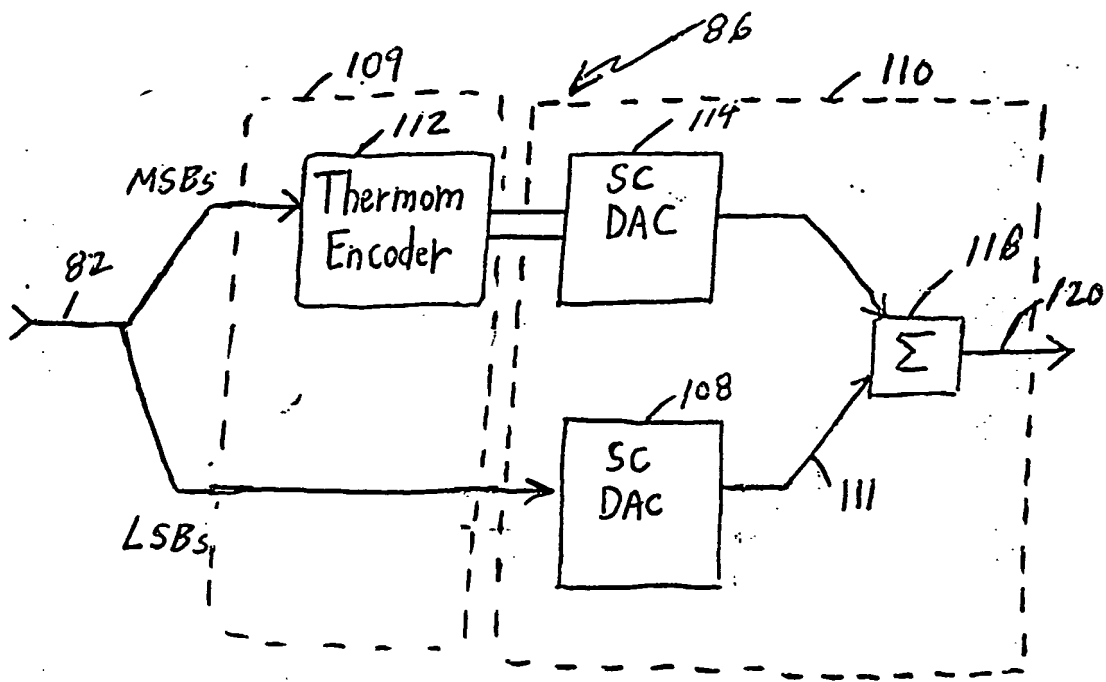


FIG. 3

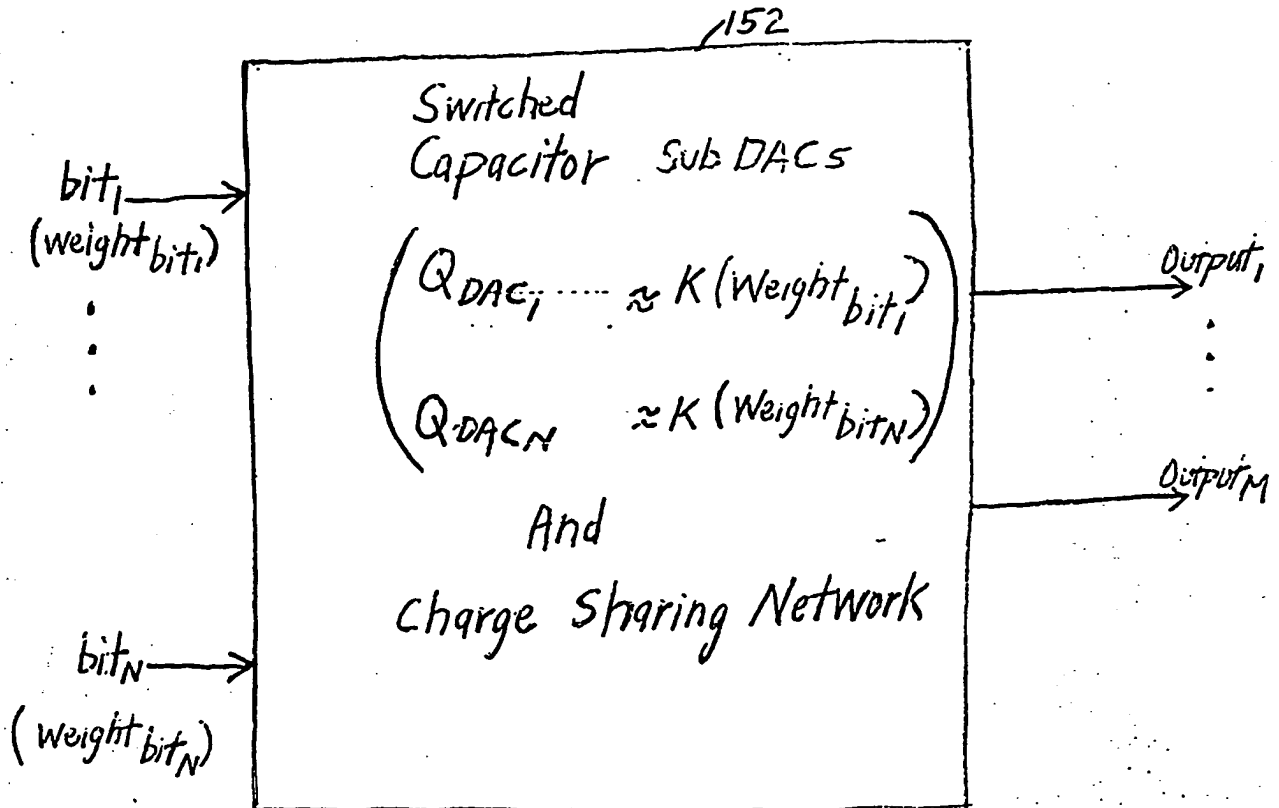


FIG. 4

FIG. 5 is a schematic diagram of a 4-bit digital-to-analog converter (DAC) circuit. The circuit is enclosed in a dashed box 150. It consists of four 1-bit DACs (162, 164, 166, 168) and four capacitors (C1, C2, C3, C4). Each 1-bit DAC is connected to a corresponding bit input (bit1, bit2, bit3, bit4) and a common output line 160. The output line 160 is connected to an output terminal 160. The circuit is controlled by a set of control signals P1, P2, and P3, which are shown in FIG. 6. The control signals P1, P2, and P3 are used to select the output of the DACs and to charge the capacitors. The output of the DACs is the sum of the weighted inputs, which is then converted to an analog signal by the capacitors. The output of the capacitors is the sum of the weighted inputs, which is then converted to an analog signal by the capacitors.

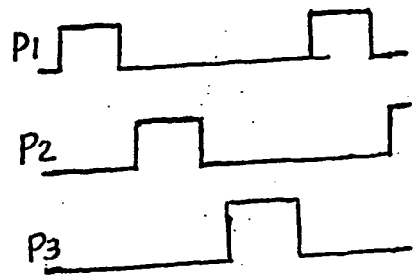
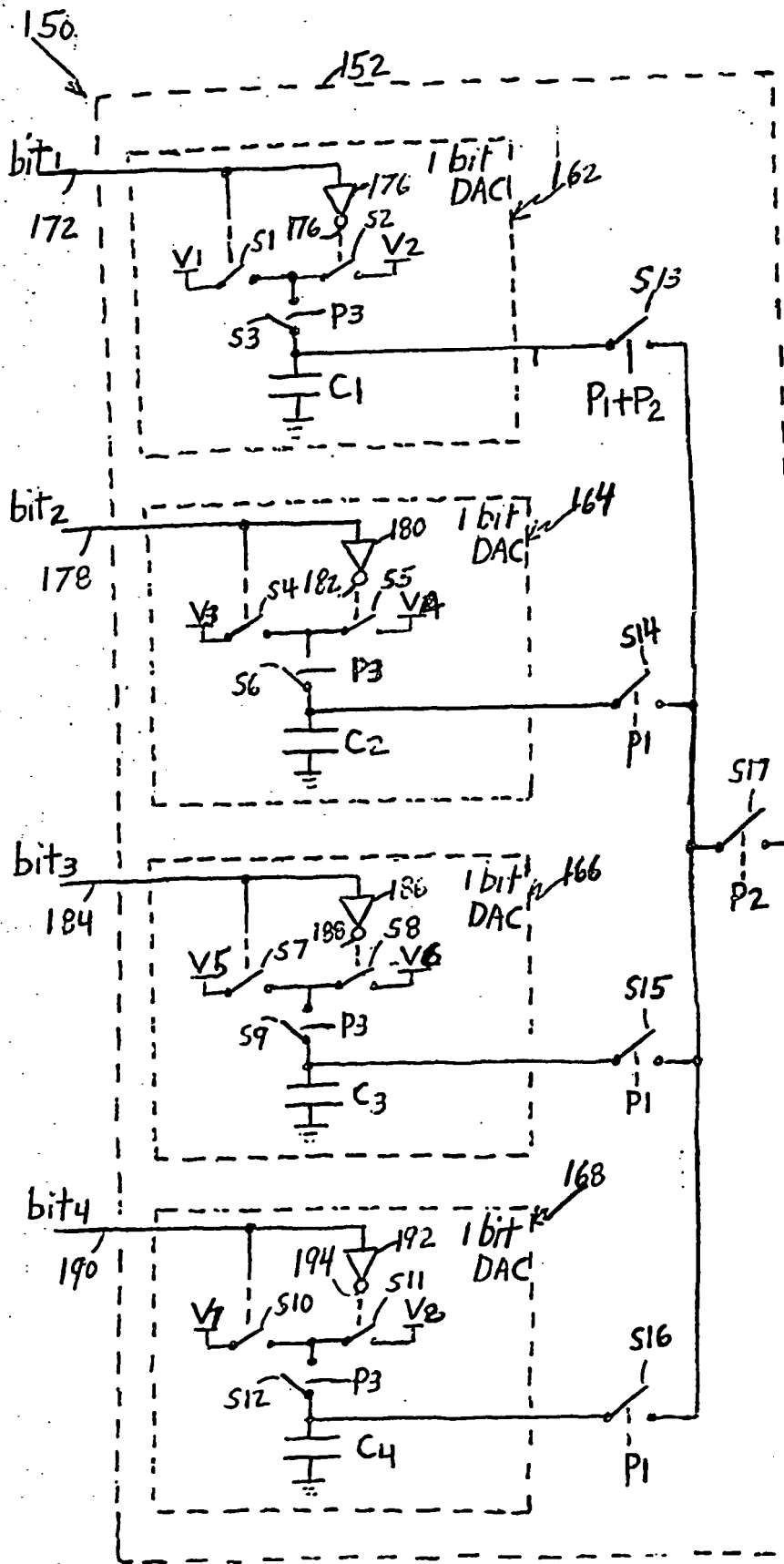
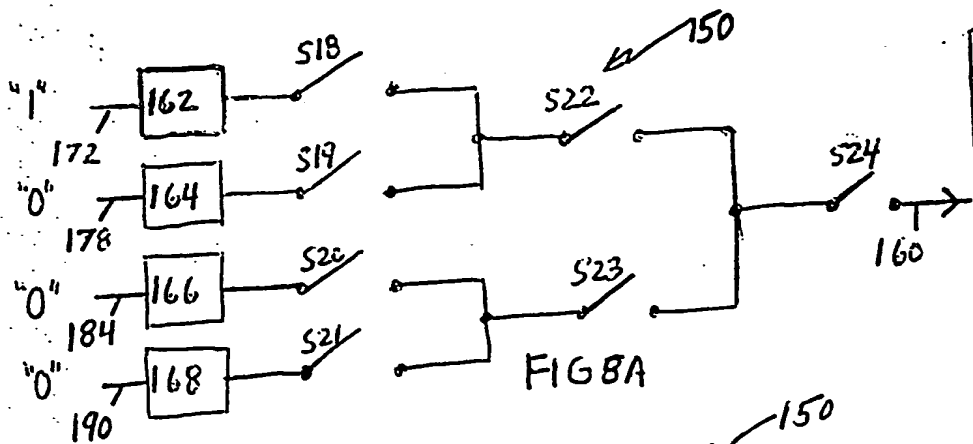
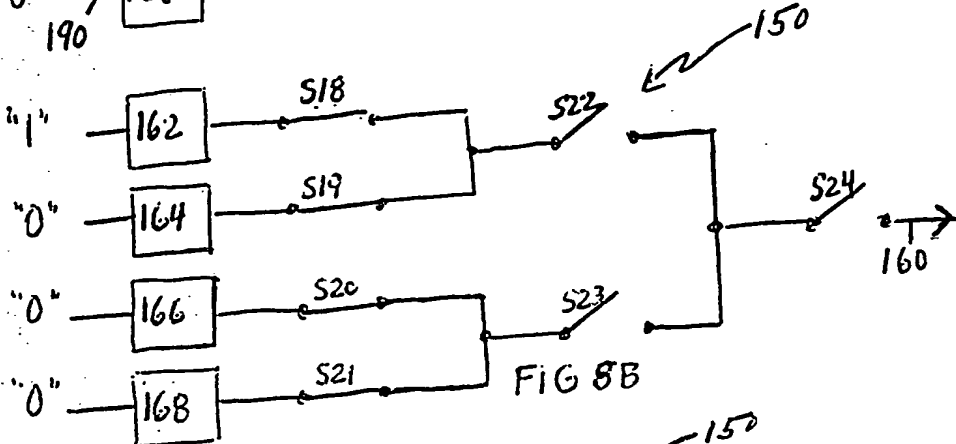


FIG. 6

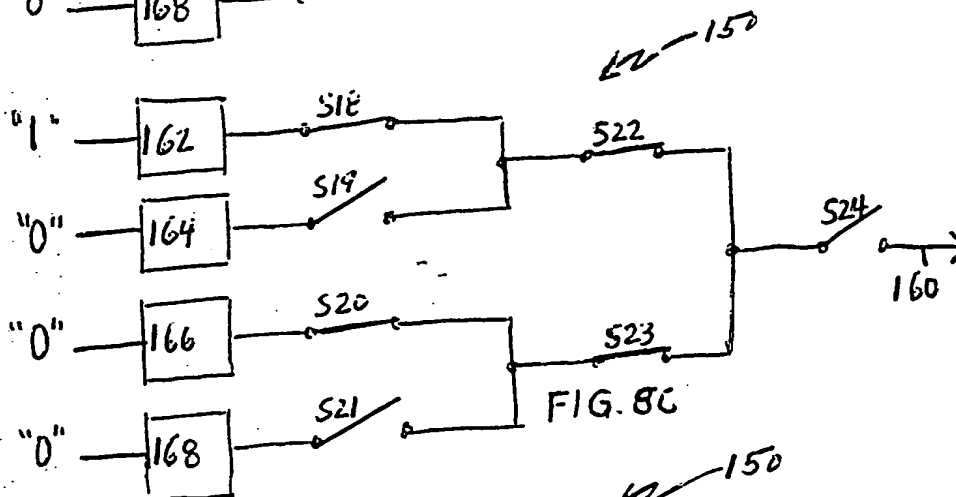
FIG. 5



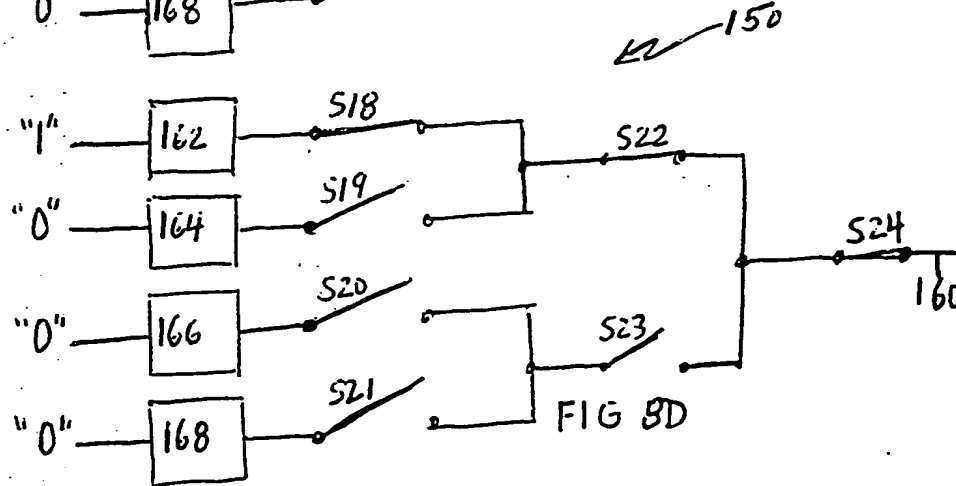
$P1=0$	$V(C1)=V_{ref}$	$Q(C1)=C \cdot V_{ref}$
$P2=0$	$V(C2)=0$	$Q(C2)=0$
$P3=1$	$V(C3)=0$	$Q(C3)=0$
$P4=0$	$V(C4)=0$	$Q(C4)=0$



$P1=0$	$V(C1)=V_{ref}/2$	$Q(C1)=C \cdot V_{ref}/2$
$P2=0$	$V(C2)=V_{ref}/2$	$Q(C2)=C \cdot V_{ref}/2$
$P3=0$	$V(C3)=0$	$Q(C3)=0$
$P4=1$	$V(C4)=0$	$Q(C4)=0$



$P1=1$	$V(C1)=V_{ref}/4$	$Q(C1)=C \cdot V_{ref}/4$
$P2=0$	$V(C2)=V_{ref}/2$	$Q(C2)=C \cdot V_{ref}/2$
$P3=0$	$V(C3)=V_{ref}/4$	$Q(C3)=C \cdot V_{ref}/4$
$P4=0$	$V(C4)=0$	$Q(C4)=0$



$P1=0$	$V(C1)=V_{ref}/4$	$Q(C1)=C \cdot V_{ref}/4$
$P2=1$	$V(C2)=V_{ref}/2$	$Q(C2)=C \cdot V_{ref}/2$
$P3=0$	$V(C3)=V_{ref}/4$	$Q(C3)=C \cdot V_{ref}/4$
$P4=0$	$V(C4)=0$	$Q(C4)=0$

Master
Clock

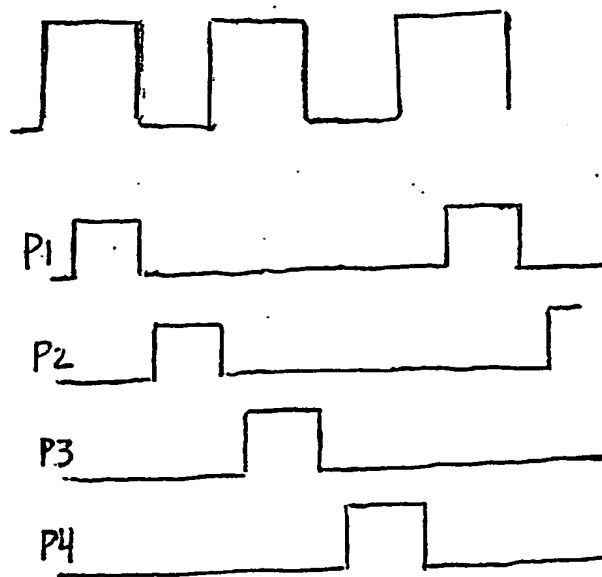


FIG 9

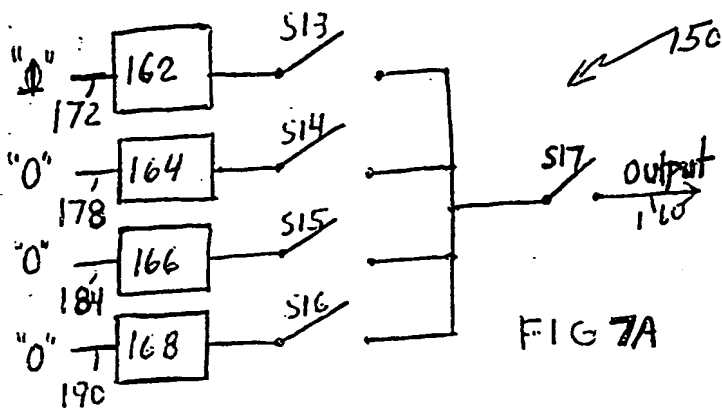


FIG 7A

P1 "0"	$V(C_1) = V_{ref}$	$Q(C_1) = C \cdot V_{ref}$
P2 "0"	$V(C_2) = 0$	$Q(C_2) = 0$
P3 "1"	$V(C_3) = 0$	$Q(C_3) = 0$
	$V(C_4) = 0$	$Q(C_4) = 0$

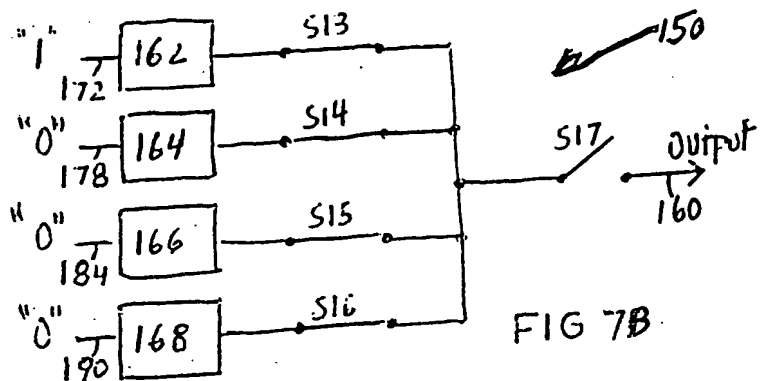


FIG 7B

P1 "1"	$V(C_1) = V_{ref}/4$	$Q(C_1) = C \cdot V_{ref}/4$
P2 "0"	$V(C_2) = V_{ref}/4$	$Q(C_2) = C \cdot V_{ref}/4$
P3 "0"	$V(C_3) = V_{ref}/4$	$Q(C_3) = C \cdot V_{ref}/4$
	$V(C_4) = V_{ref}/4$	$Q(C_4) = C \cdot V_{ref}/4$

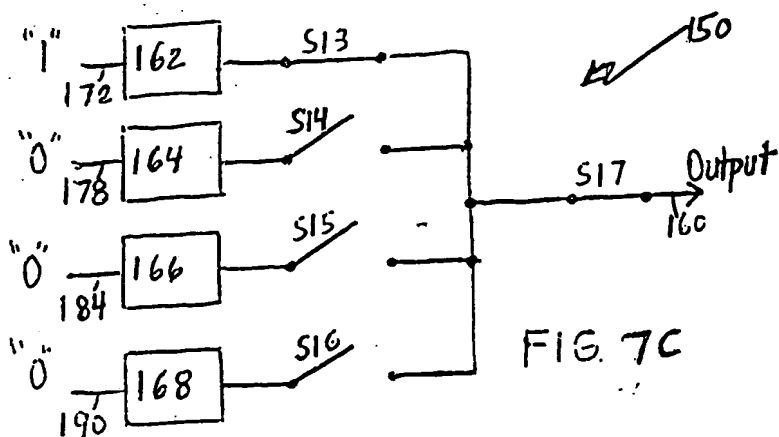


FIG 7C

P1 "0"	$V(C_1) = V_{ref}/4$	$Q(C_1) = C \cdot V_{ref}/4$
P2 "1"	$V(C_2) = V_{ref}/4$	$Q(C_2) = C \cdot V_{ref}/4$
P3 "0"	$V(C_3) = V_{ref}/4$	$Q(C_3) = C \cdot V_{ref}/4$
	$V(C_4) = V_{ref}/4$	$Q(C_4) = C \cdot V_{ref}/4$

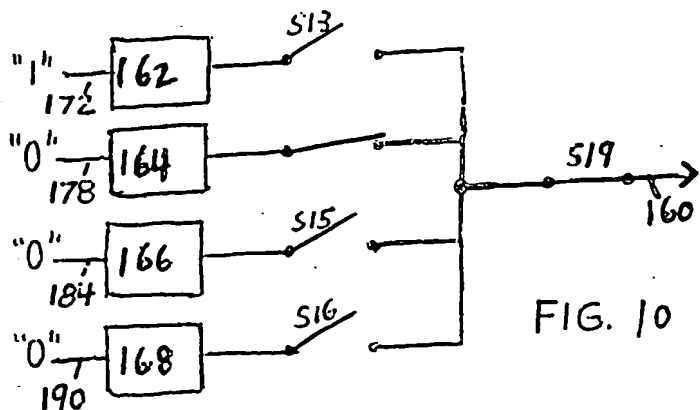
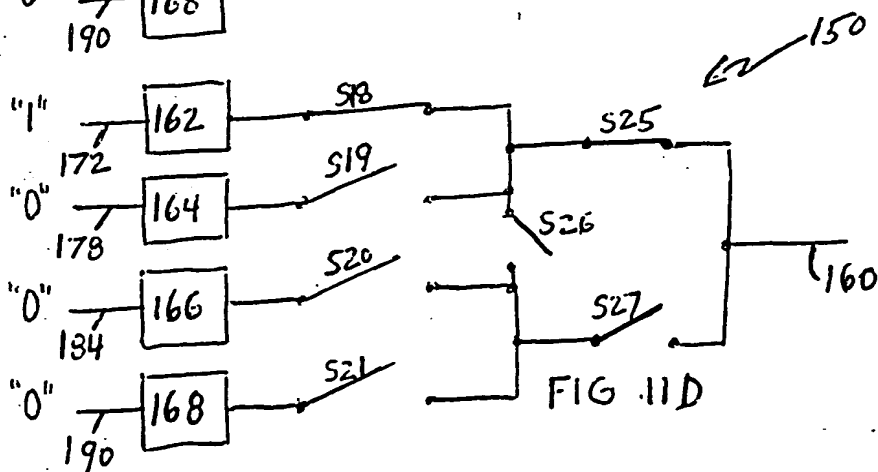
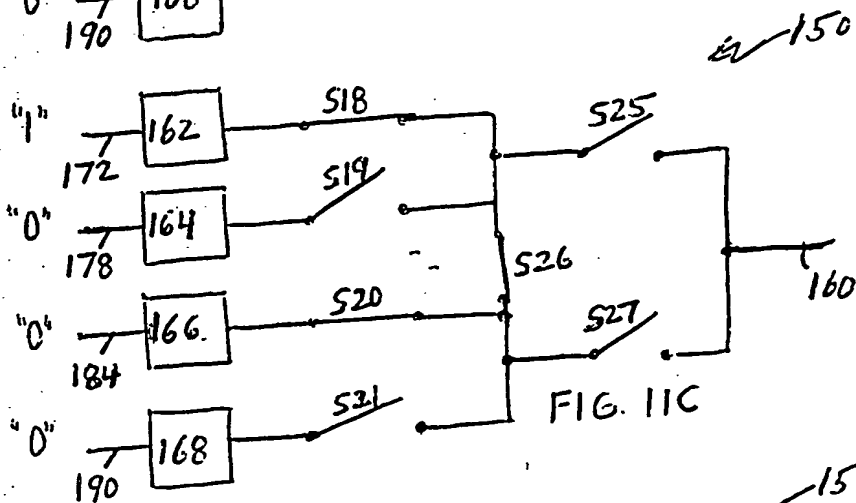
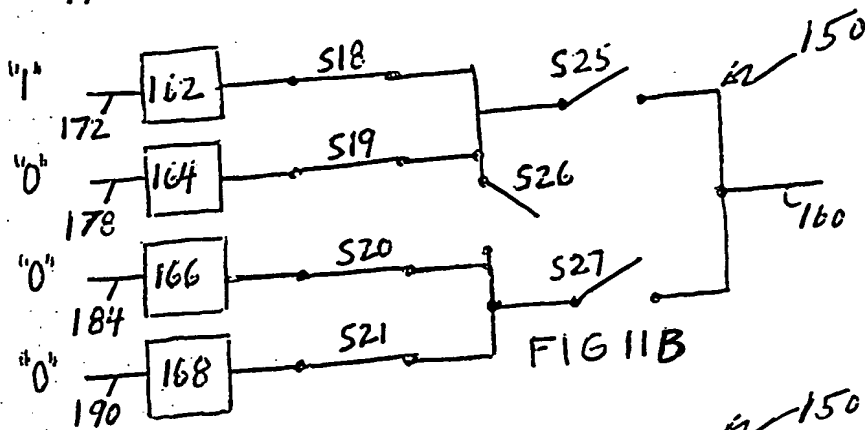
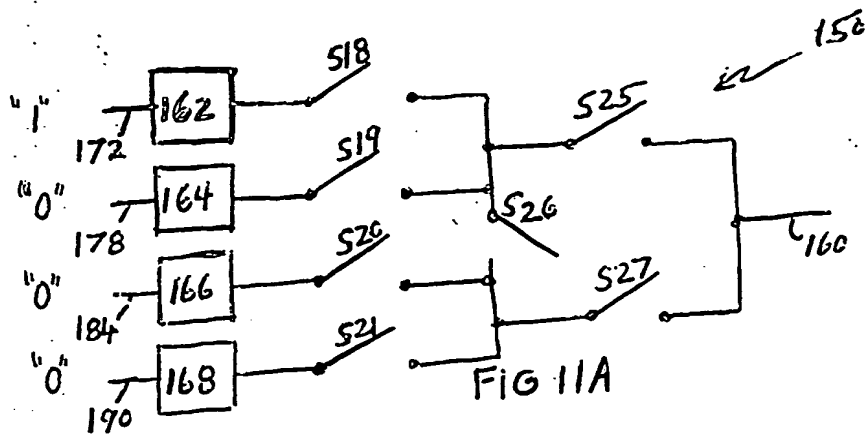
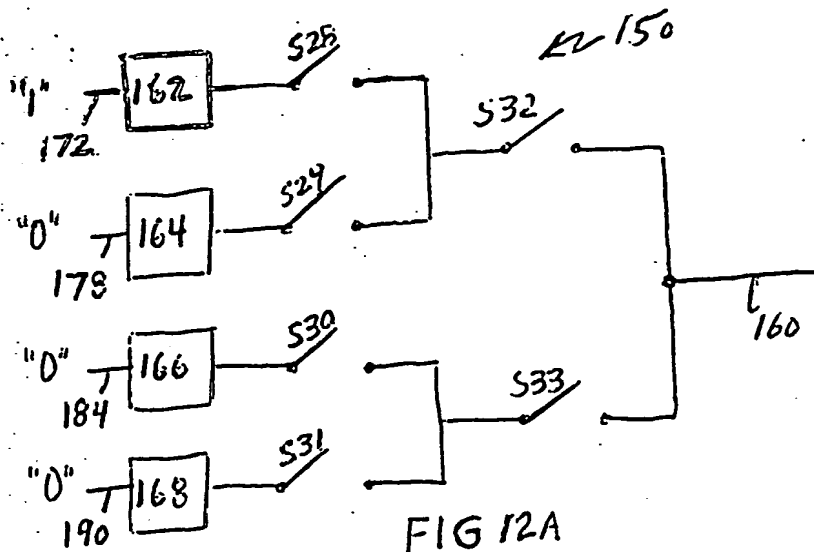
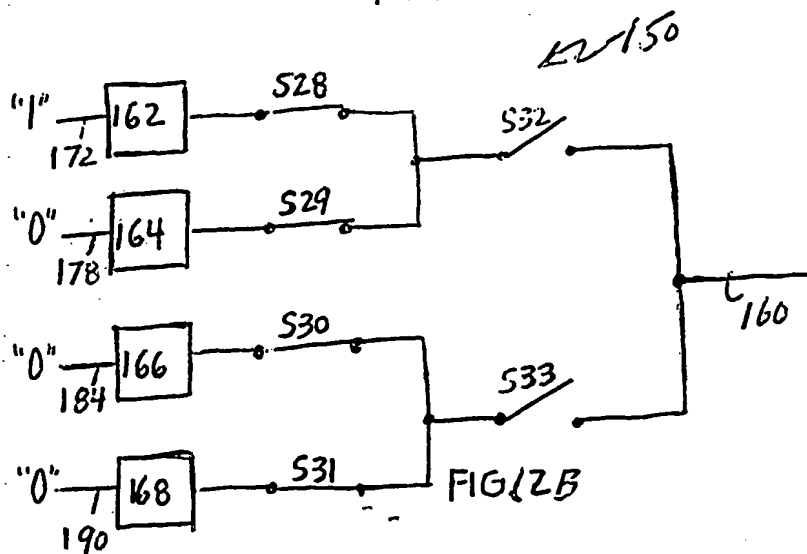


FIG. 10

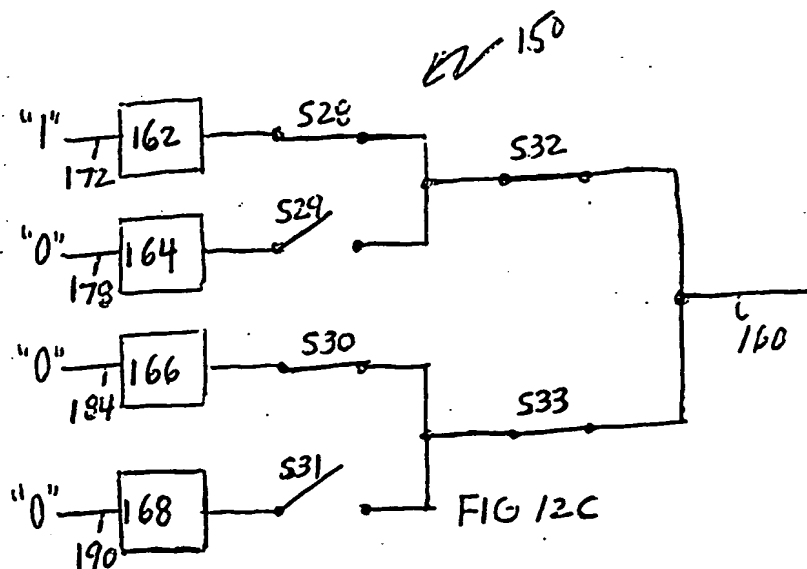




$P1=0$	$V(C1)=V_{ref}$	$Q(C1)=C \cdot V_{ref}$
$P2=0$	$V(C2)=0$	$Q(C2)=0$
$P3=1$	$V(C3)=0$	$Q(C3)=0$
	$V(C4)=0$	$Q(C4)=0$



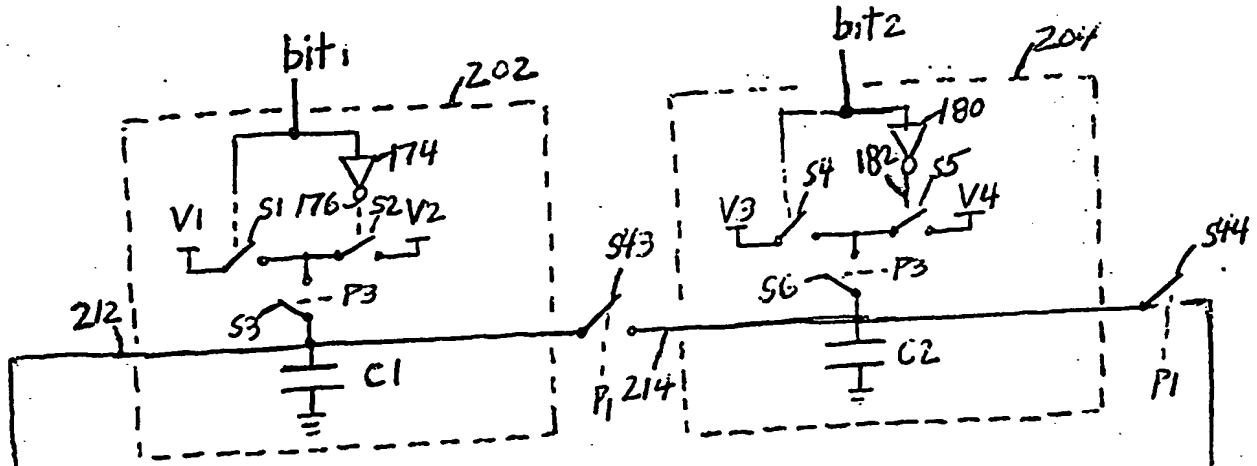
$P1=1$	$V(C1)=V_{ref}/2$	$Q(C1)=C \cdot V_{ref}/2$
$P2=0$	$V(C2)=V_{ref}/2$	$Q(C2)=C \cdot V_{ref}/2$
$P3=0$	$V(C3)=0$	$Q(C3)=0$
	$V(C4)=0$	$Q(C4)=0$



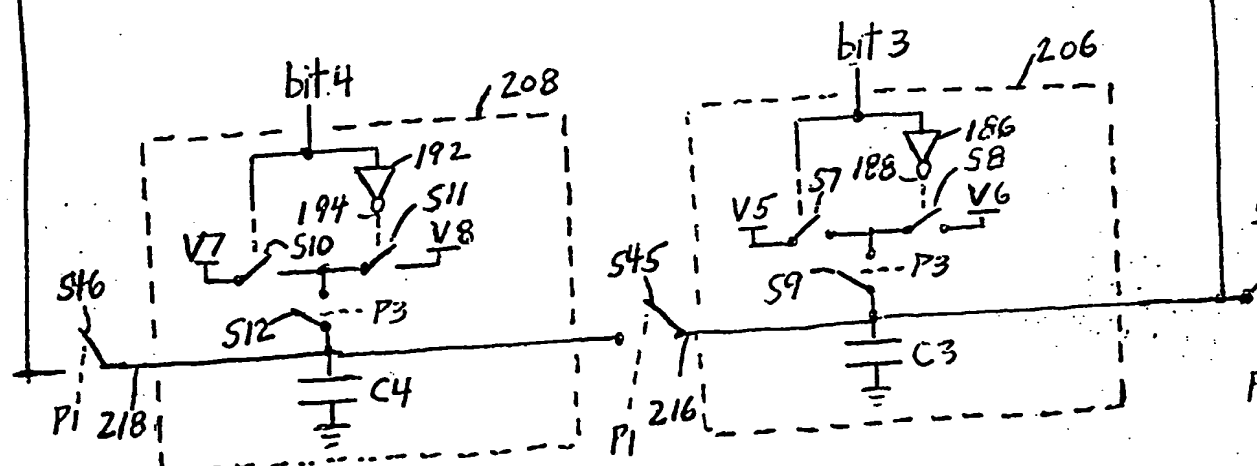
$P1=0$	$V(C1)=V_{ref}/2$	$Q(C1)=C \cdot V_{ref}/2$
$P2=1$	$V(C2)=V_{ref}/2$	$Q(C2)=C \cdot V_{ref}/2$
$P3=0$	$V(C3)=0$	$Q(C3)=0$
	$V(C4)=0$	$Q(C4)=0$

150 152

bit1
172
bit2
178

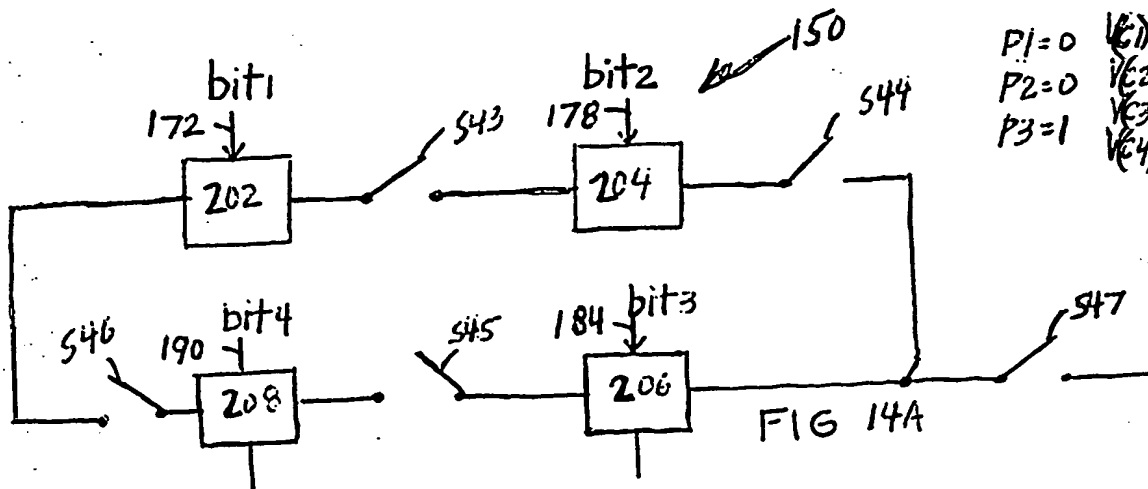


bit3
184

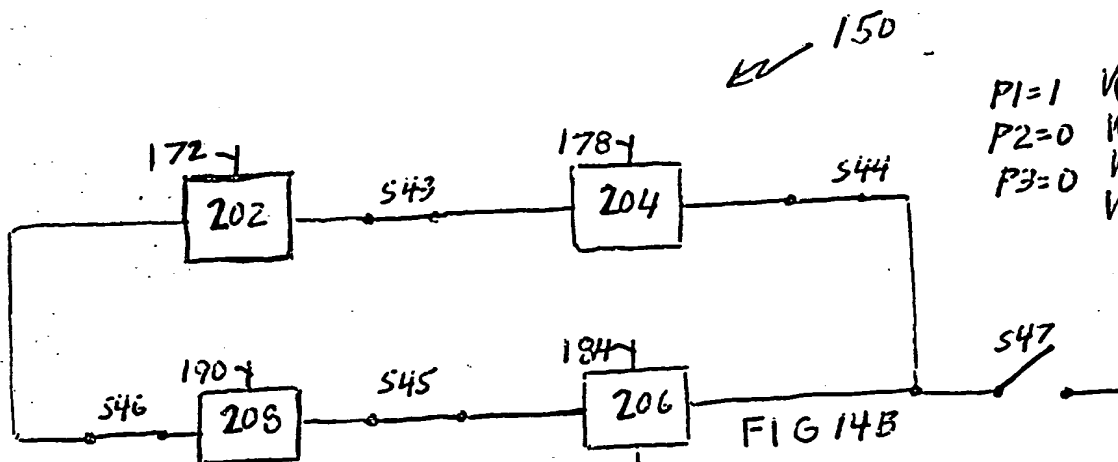


bit4
190

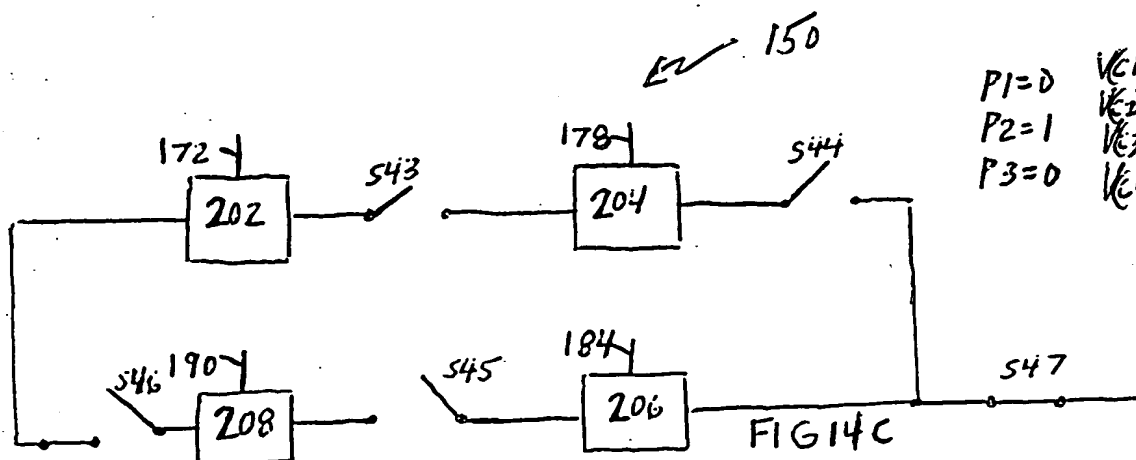
FIG. 13



$$\begin{array}{l}
 P1=0 \quad V(C1)=V_{ref} \quad Q(C1)=C \times V_{ref} \\
 P2=0 \quad V(C2)=0 \quad Q(C2)=0 \\
 P3=1 \quad V(C3)=0 \quad Q(C3)=0 \\
 \quad \quad V(C4)=0 \quad Q(C4)=0
 \end{array}$$



$$\begin{array}{l}
 P1=1 \quad V(C1)=V_{ref}/4 \quad Q(C1)=C \times V_{ref}/4 \\
 P2=0 \quad V(C2)=V_{ref}/4 \quad Q(C2)=C \times V_{ref}/4 \\
 P3=0 \quad V(C3)=V_{ref}/4 \quad Q(C3)=C \times V_{ref}/4 \\
 \quad \quad V(C4)=V_{ref}/4 \quad Q(C4)=C \times V_{ref}/4
 \end{array}$$



$$\begin{array}{l}
 P1=0 \quad V(C1)=V_{ref}/4 \quad Q(C1)=C \times V_{ref}/4 \\
 P2=1 \quad V(C2)=V_{ref}/4 \quad Q(C2)=C \times V_{ref}/4 \\
 P3=0 \quad V(C3)=V_{ref}/4 \quad Q(C3)=C \times V_{ref}/4 \\
 \quad \quad V(C4)=V_{ref}/4 \quad Q(C4)=C \times V_{ref}/4
 \end{array}$$

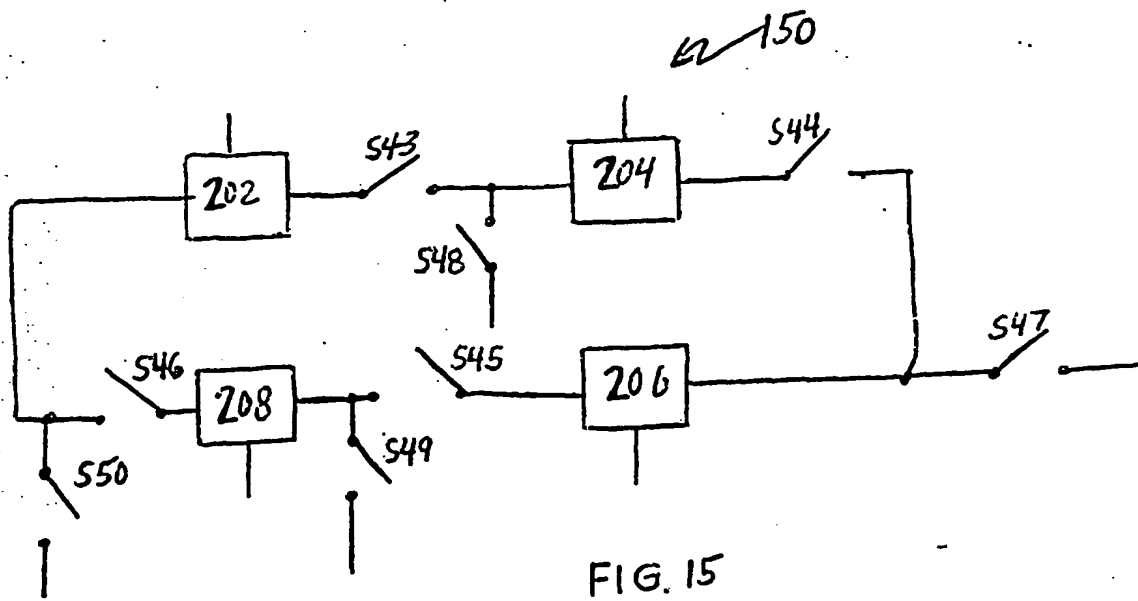


FIG 16A

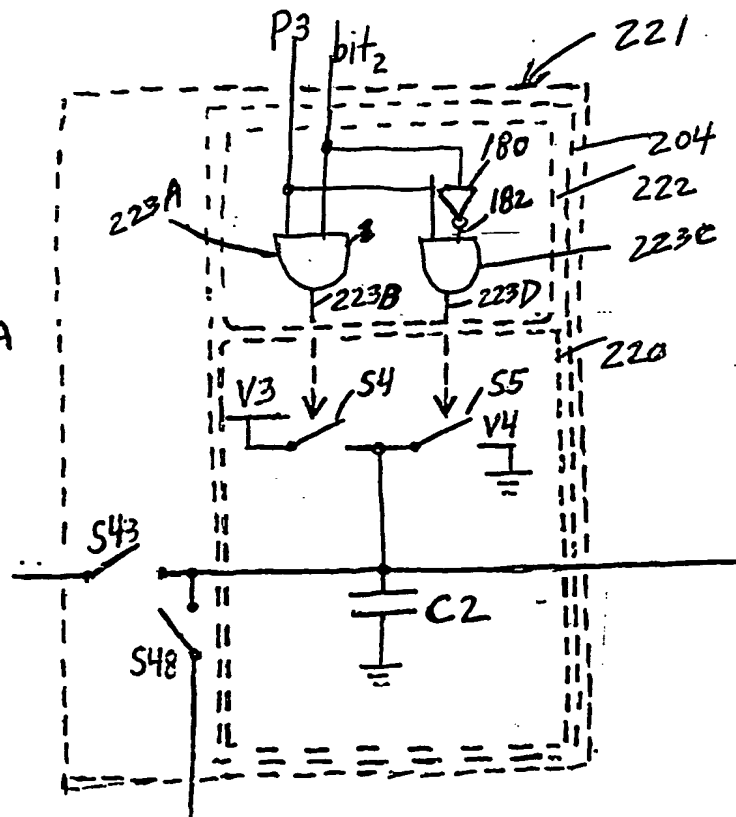
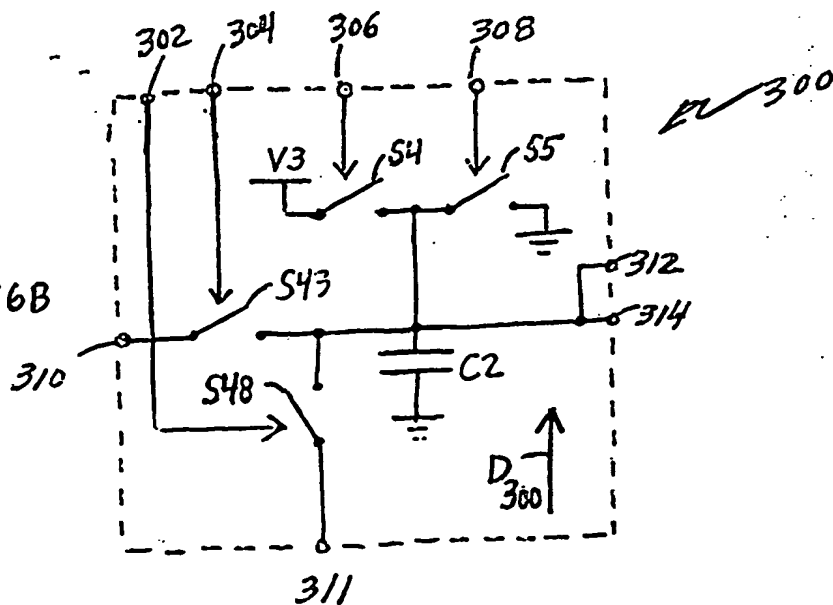
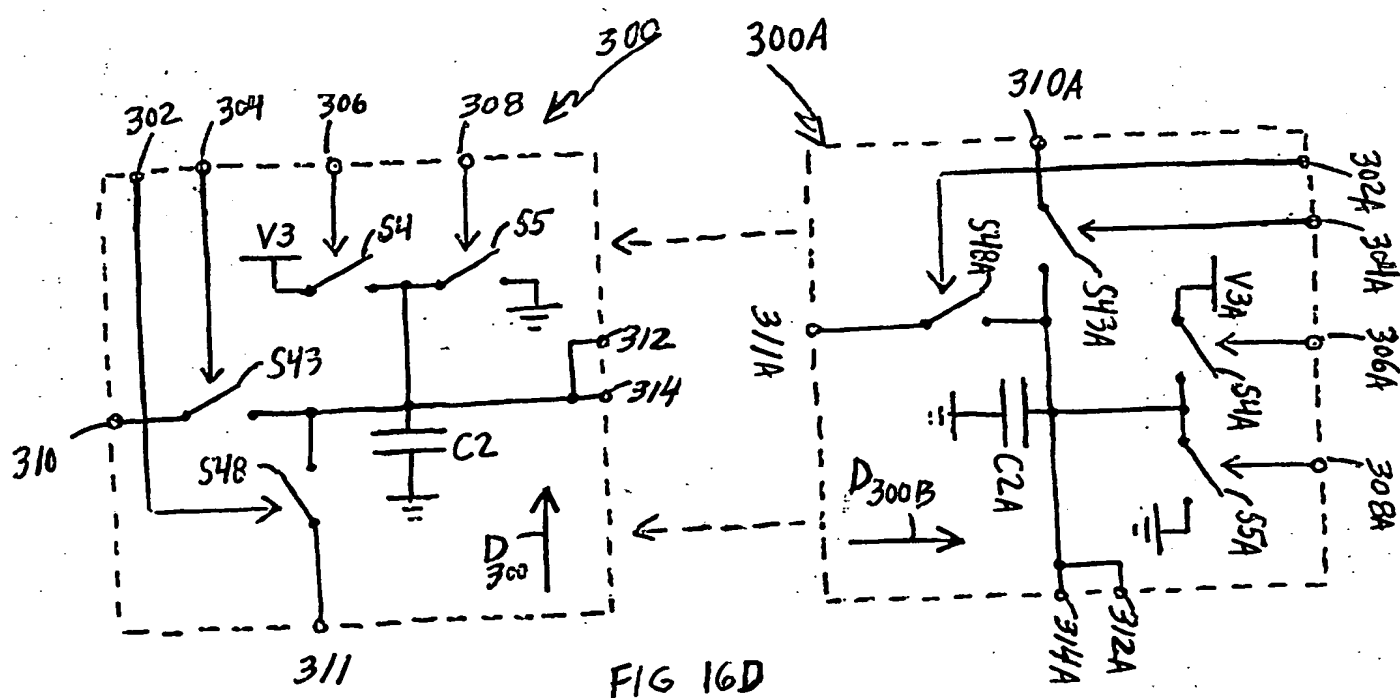
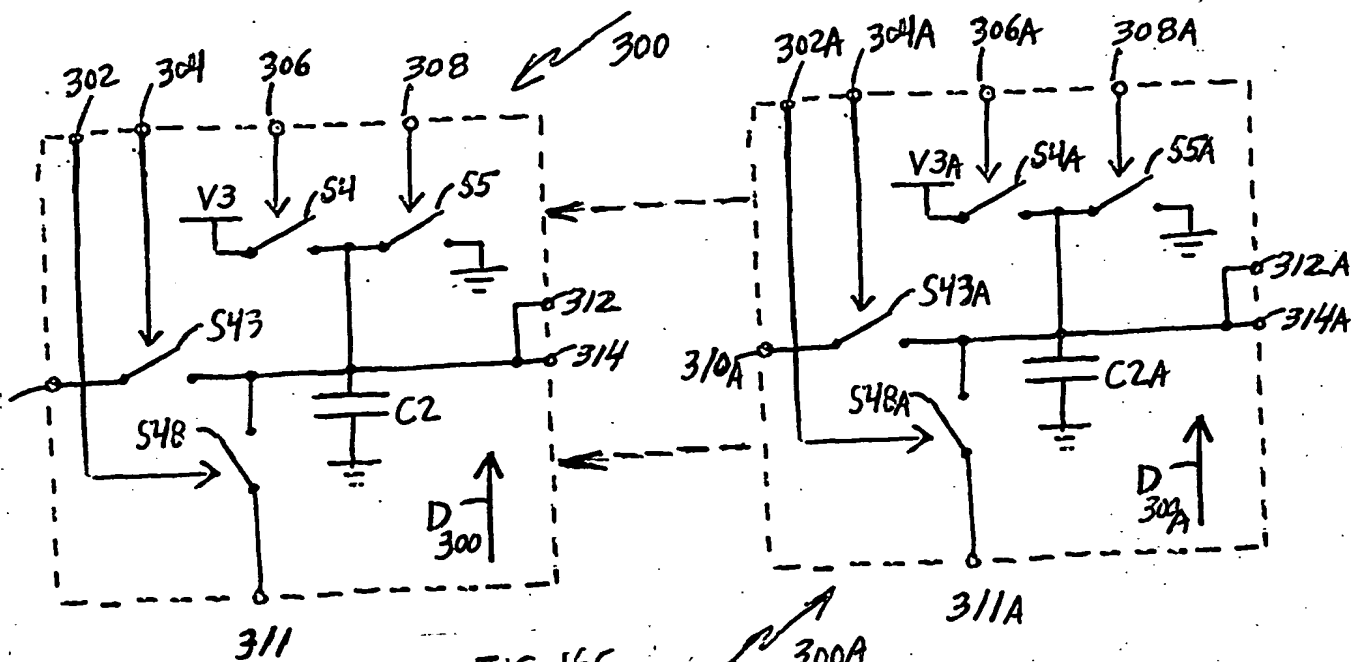
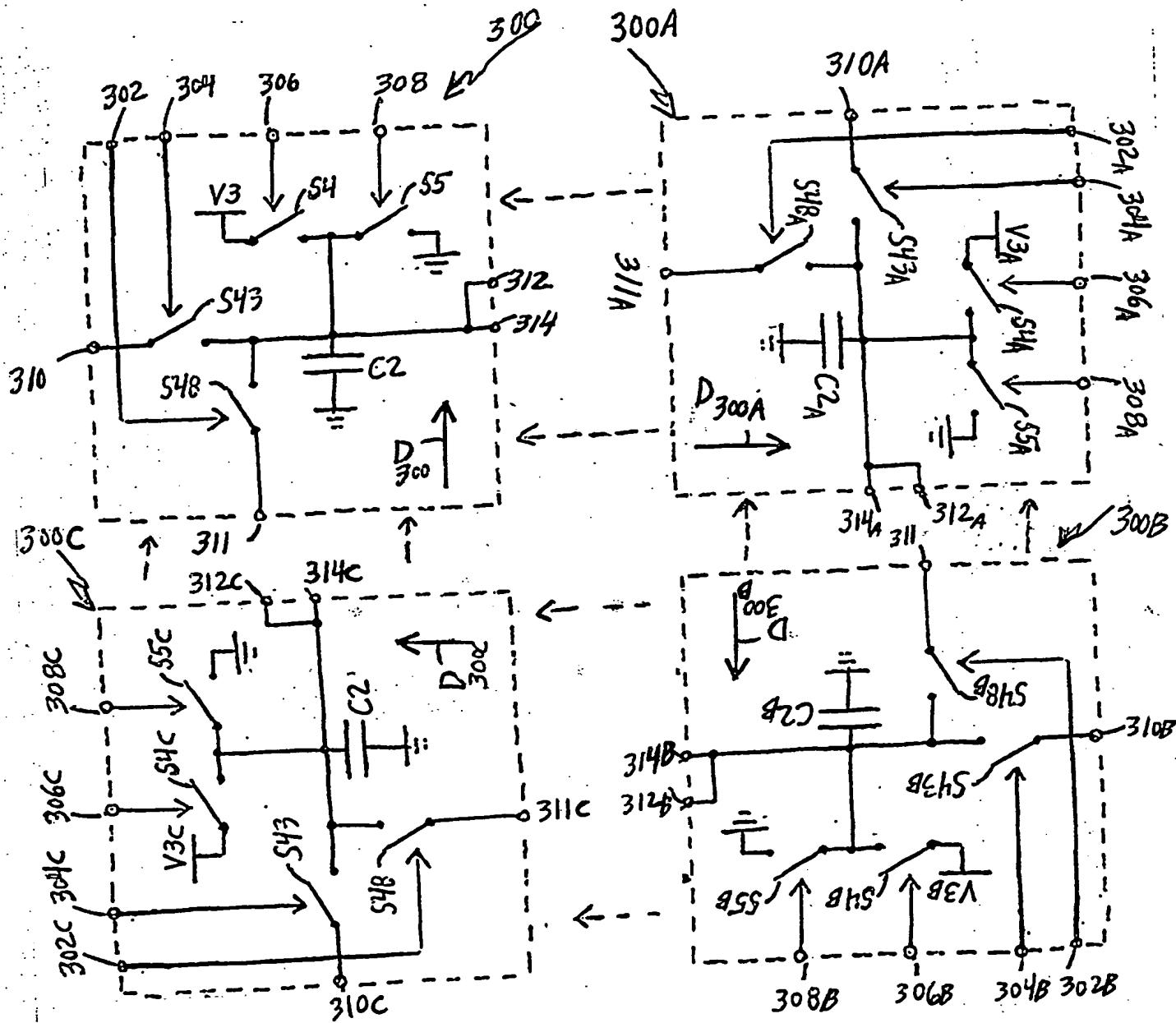


FIG 16B





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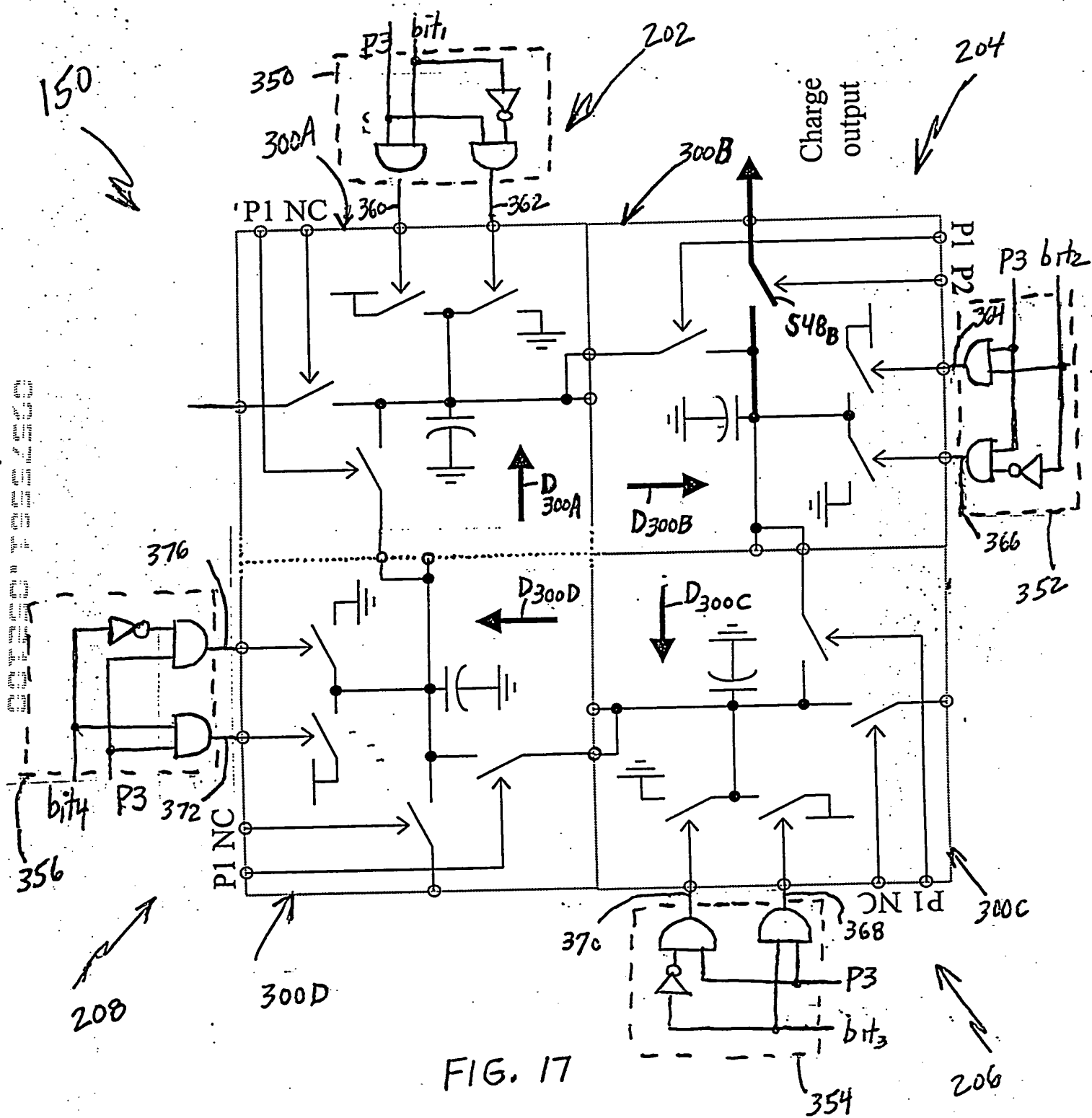


FIG. 17

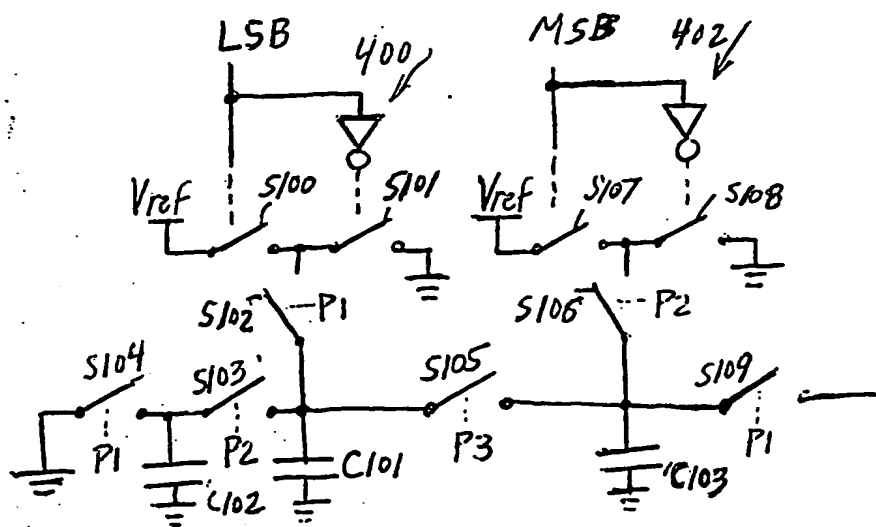
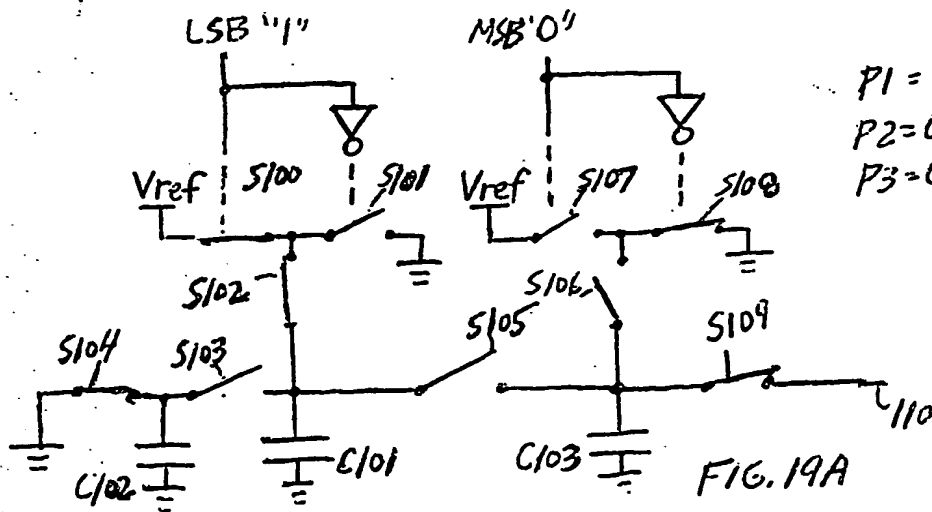
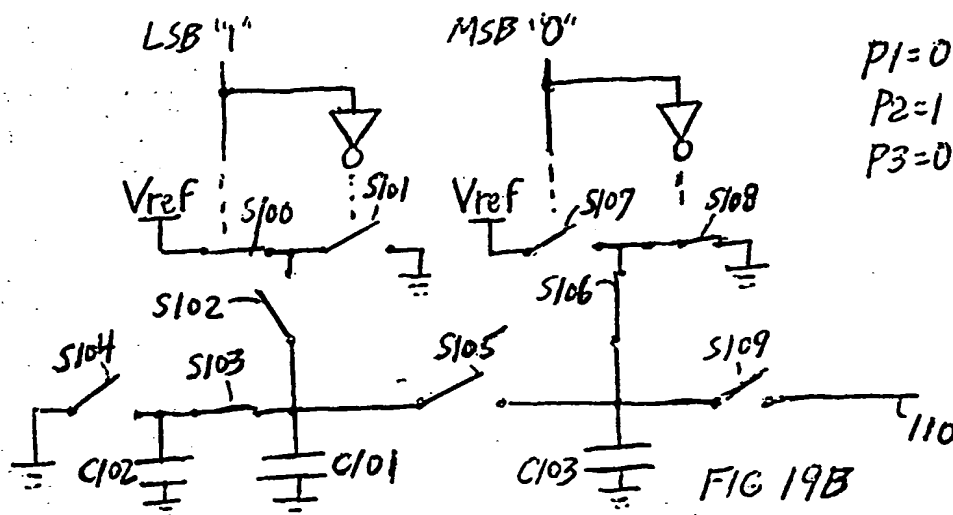


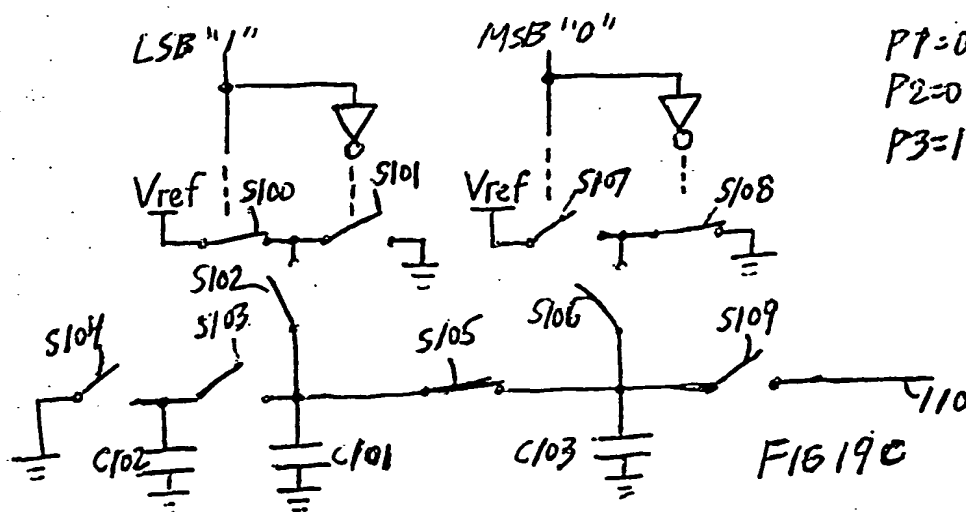
FIG. 18



$$\begin{aligned}
 P1 &= 1 & V(C102) &= 0 & Q(C102) &= 0 \\
 P2 &= 0 & V(C101) &= V_{ref} & Q(C101) &= C \cdot V_{ref} \\
 P3 &= 0 & V(C103) &= ? & Q(C103) &= ?
 \end{aligned}$$



$$\begin{aligned}
 P1 &= 0 & V(C102) &= V_{ref}/2 & Q(C102) &= C \cdot V_{ref}/2 \\
 P2 &= 1 & V(C101) &= V_{ref}/2 & Q(C101) &= C \cdot V_{ref}/2 \\
 P3 &= 0 & V(C103) &= 0 & Q(C103) &= 0
 \end{aligned}$$



$$\begin{aligned}
 P1 &= 0 & V(C102) &= V_{ref}/2 & Q(C102) &= C \cdot V_{ref}/2 \\
 P2 &= 0 & V(C101) &= V_{ref}/4 & Q(C101) &= C \cdot V_{ref}/4 \\
 P3 &= 1 & V(C103) &= V_{ref}/4 & Q(C103) &= C \cdot V_{ref}/4
 \end{aligned}$$

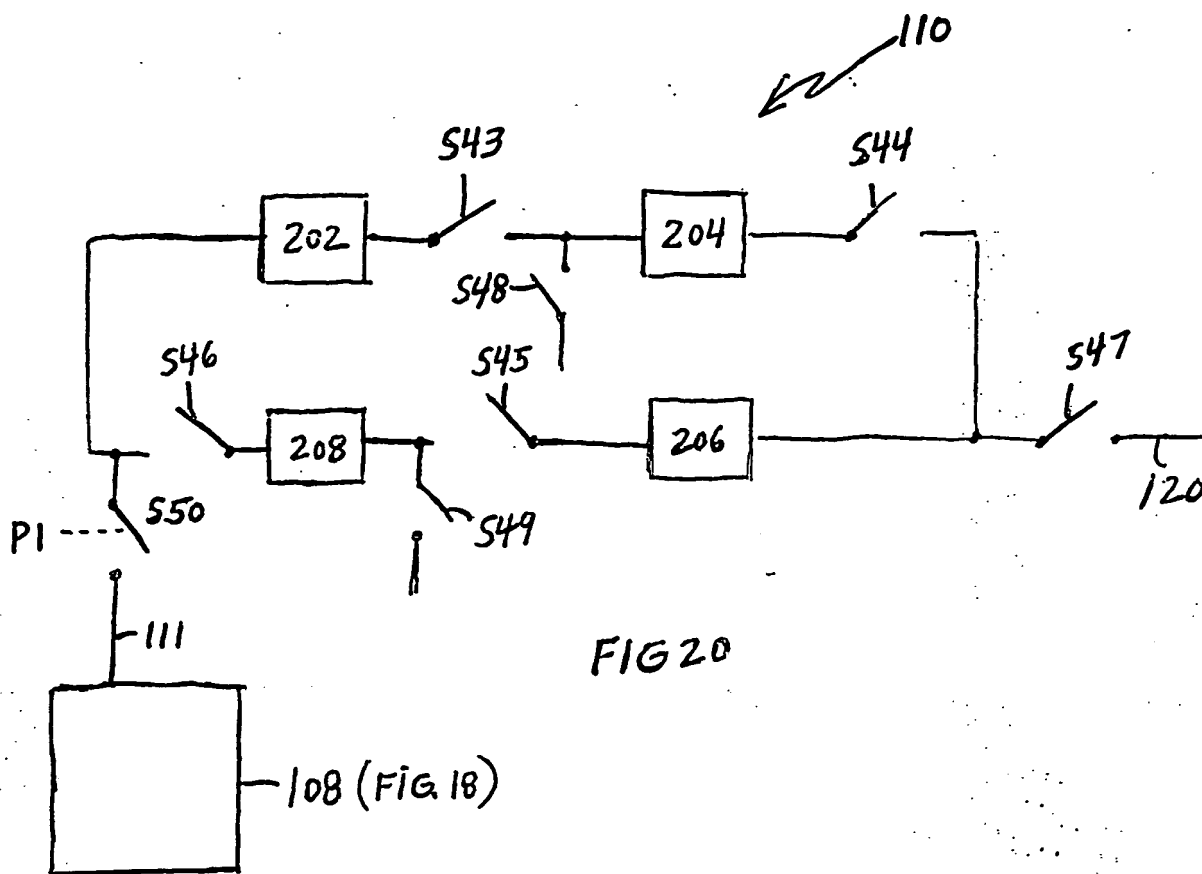


FIG 20

Hand-drawn schematic diagram of a circuit with two parallel paths. The top path contains blocks 202 and 204 with switches S43 and S44. The bottom path contains blocks 208 and 206 with switches S46, S45, and S47. A switch S48 connects the two paths between blocks 202/204 and 208/206. A switch S49 is connected to the bottom path after block 208. A switch S50 is connected to the top path before block 202. A block labeled 108 (FIG. 18) is connected to the top path via a line labeled 111. The circuit is connected to a source 110 and a terminal 120.

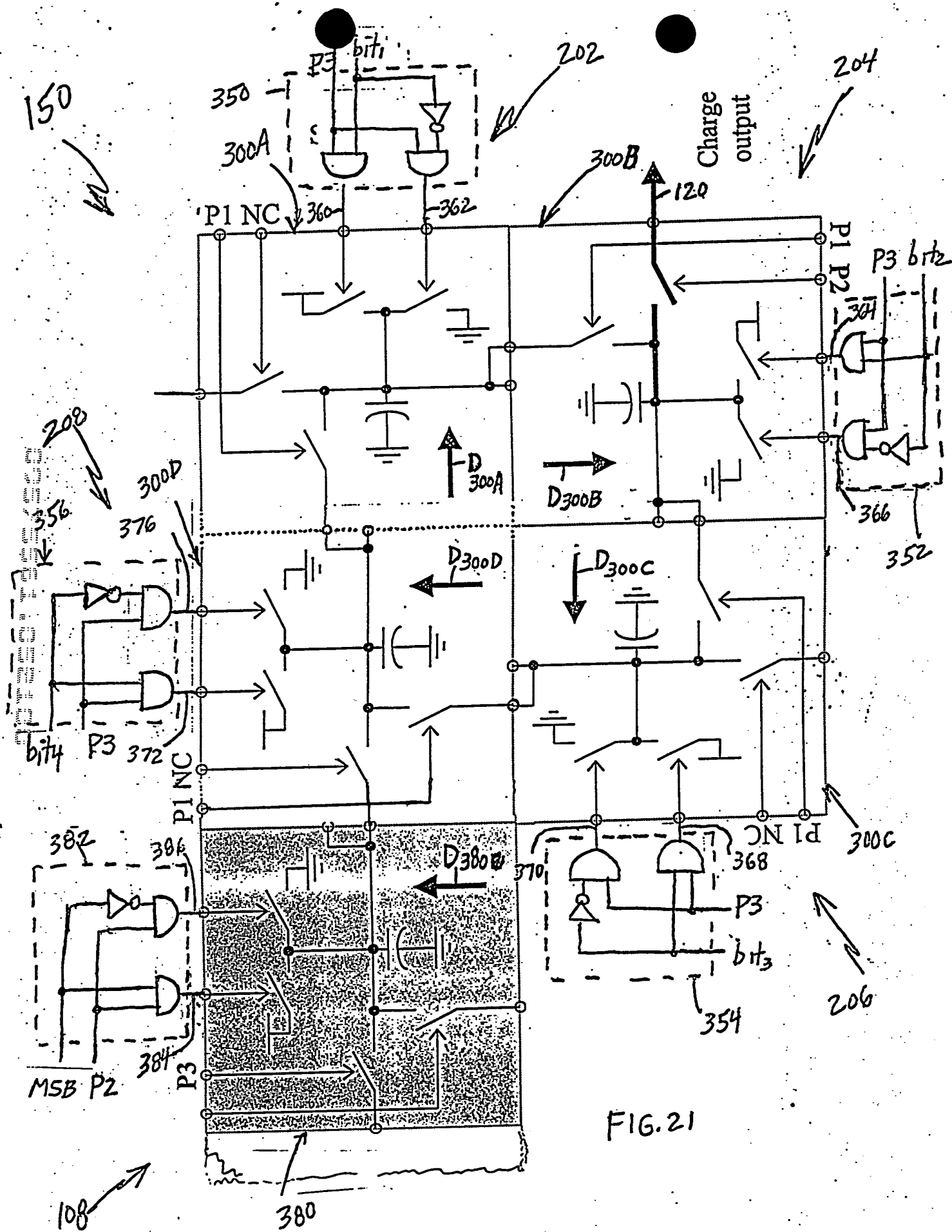


FIG. 21

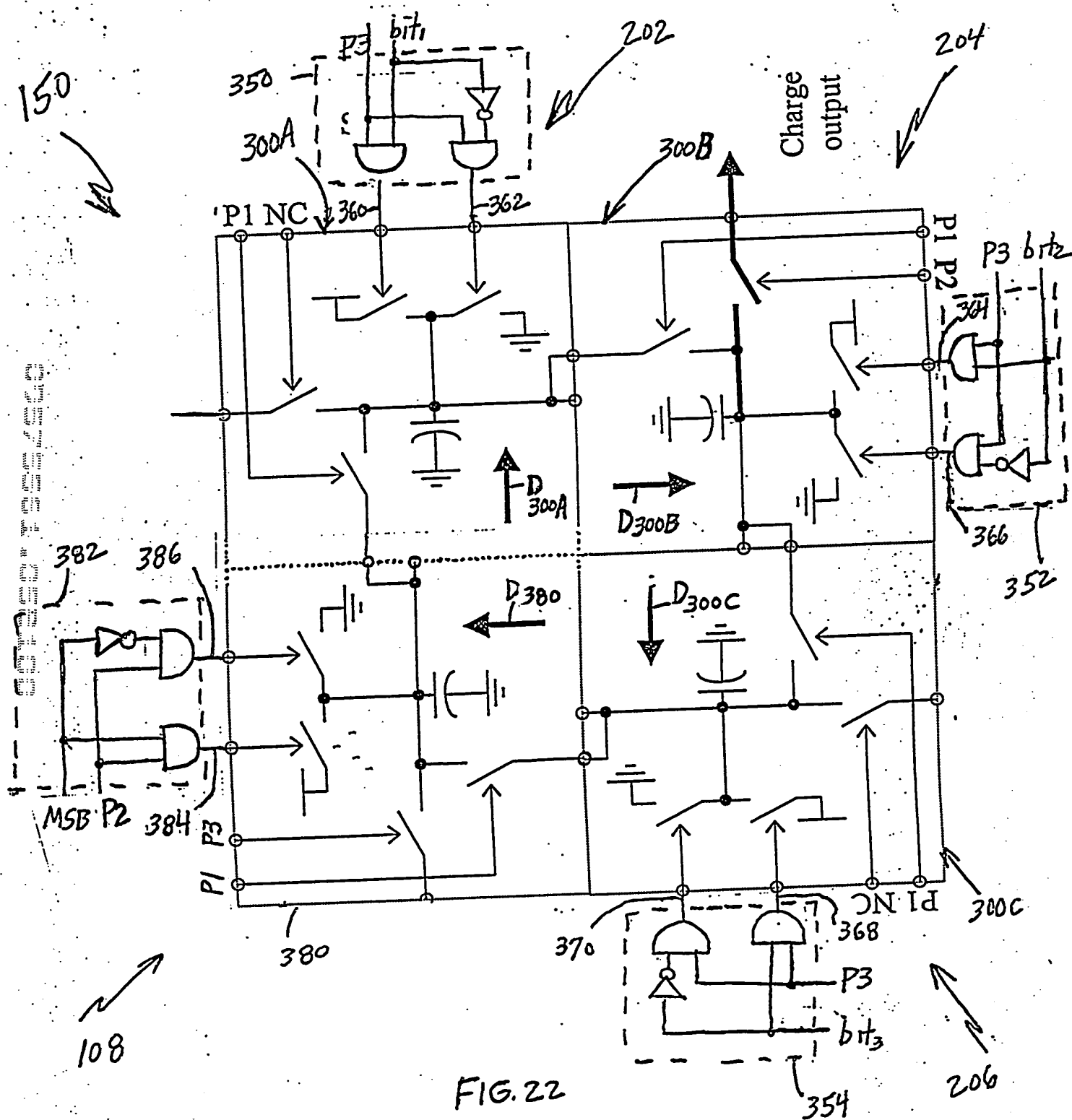


FIG. 22

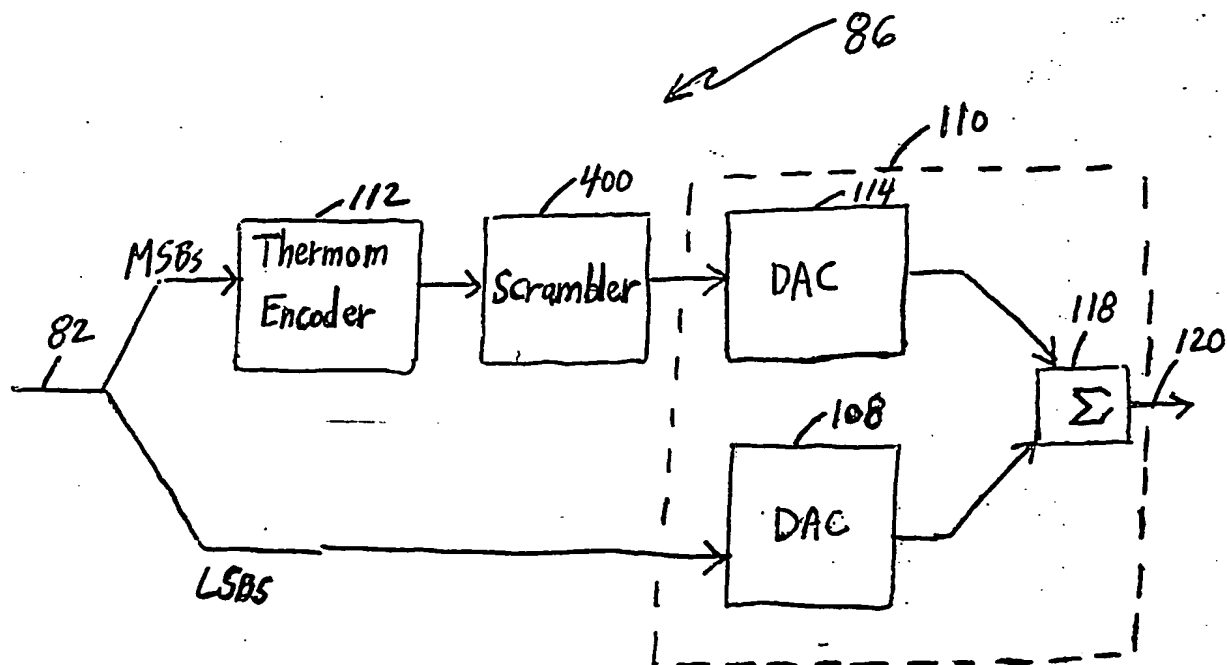


FIG. 23

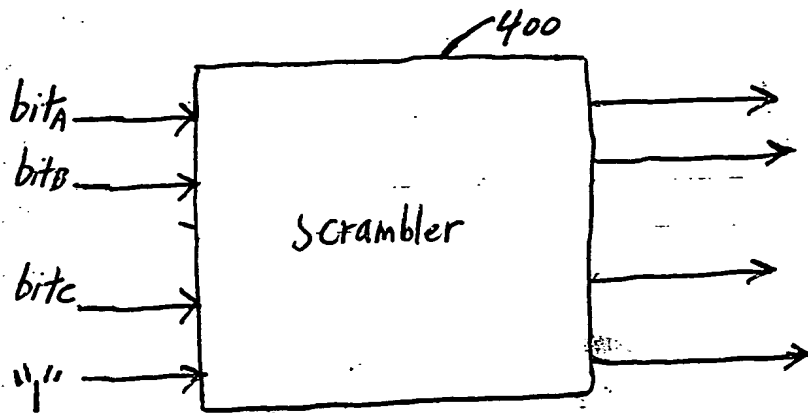


FIG 24

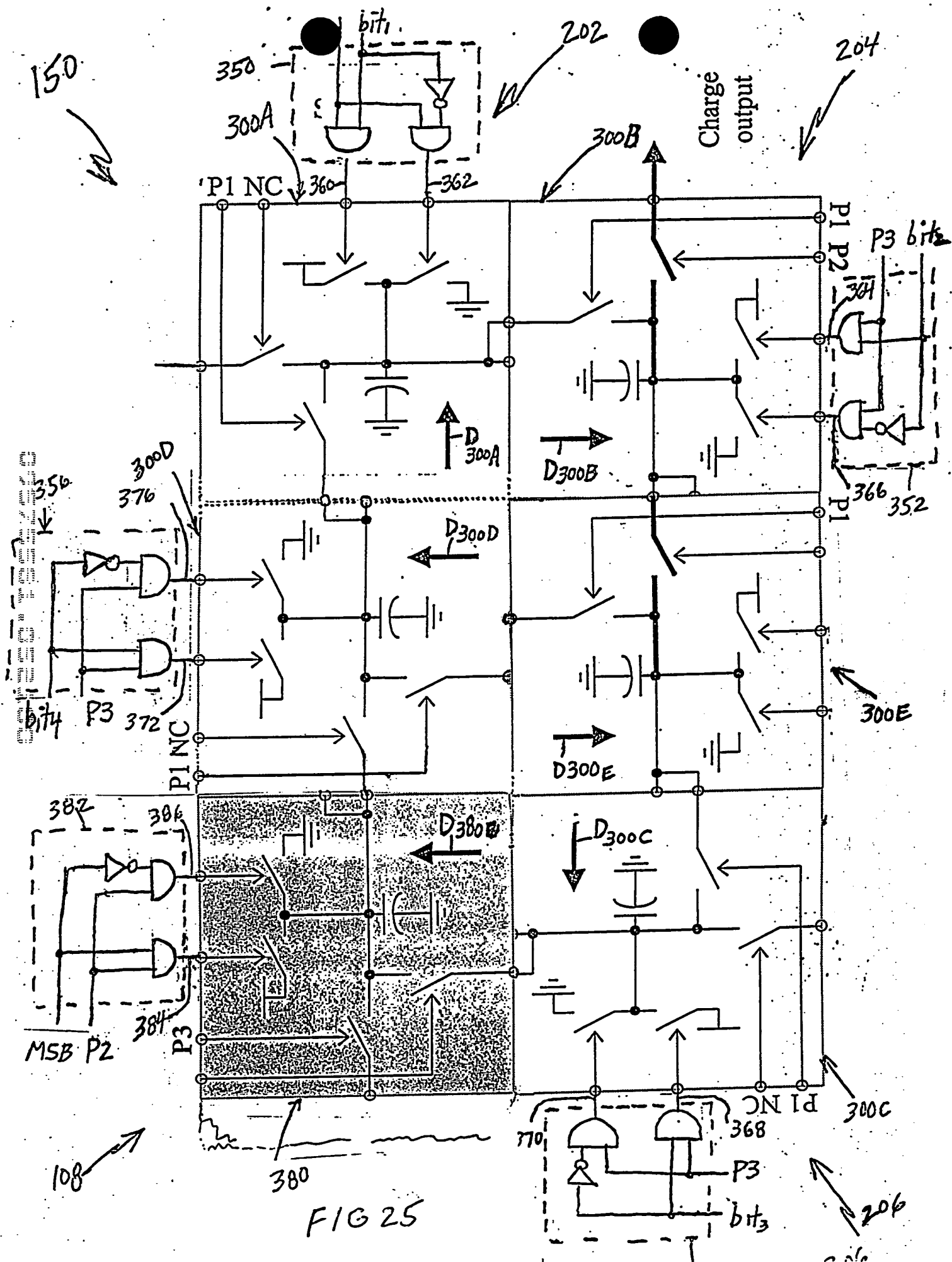


FIG 25

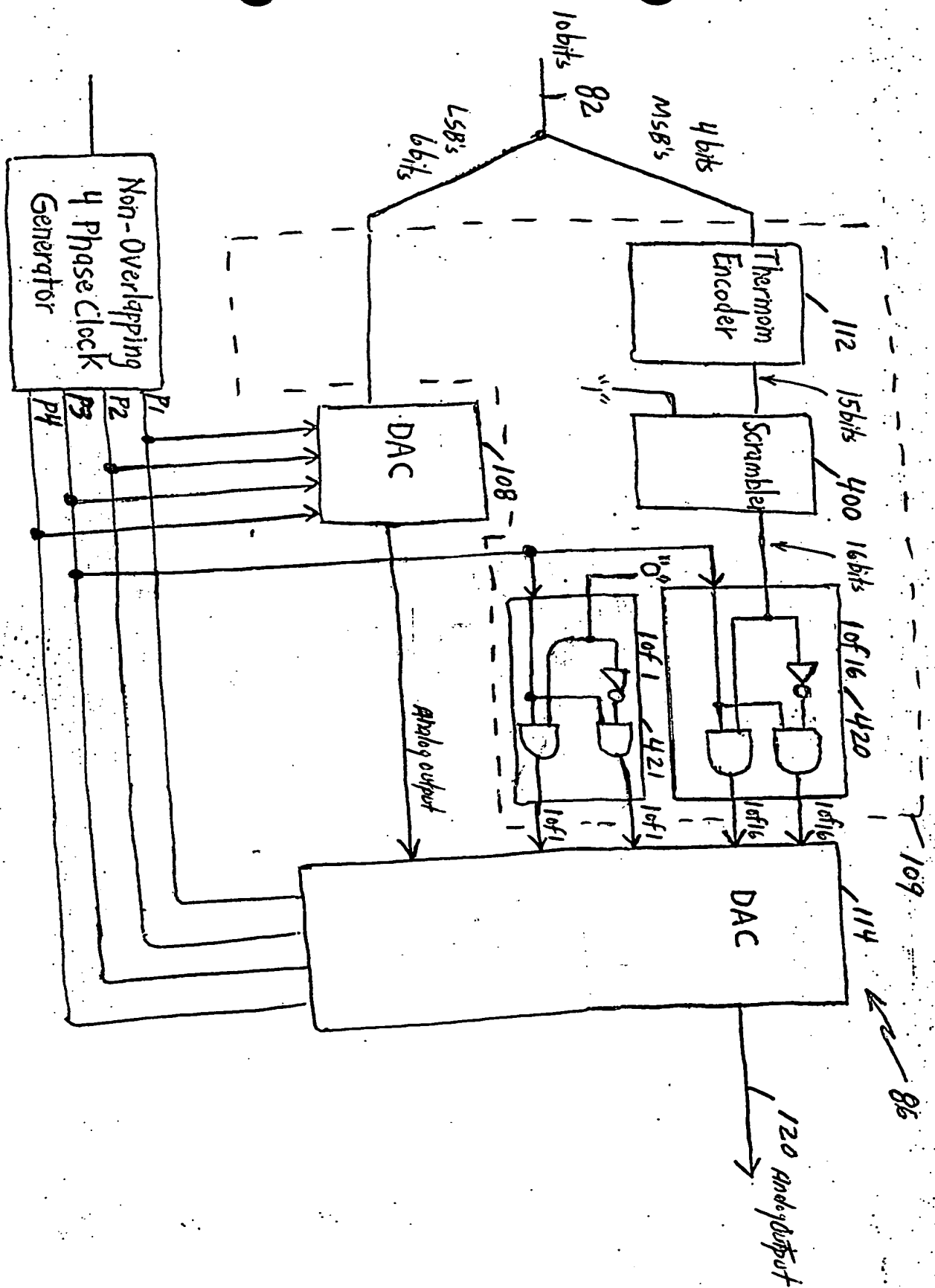
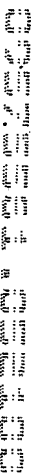
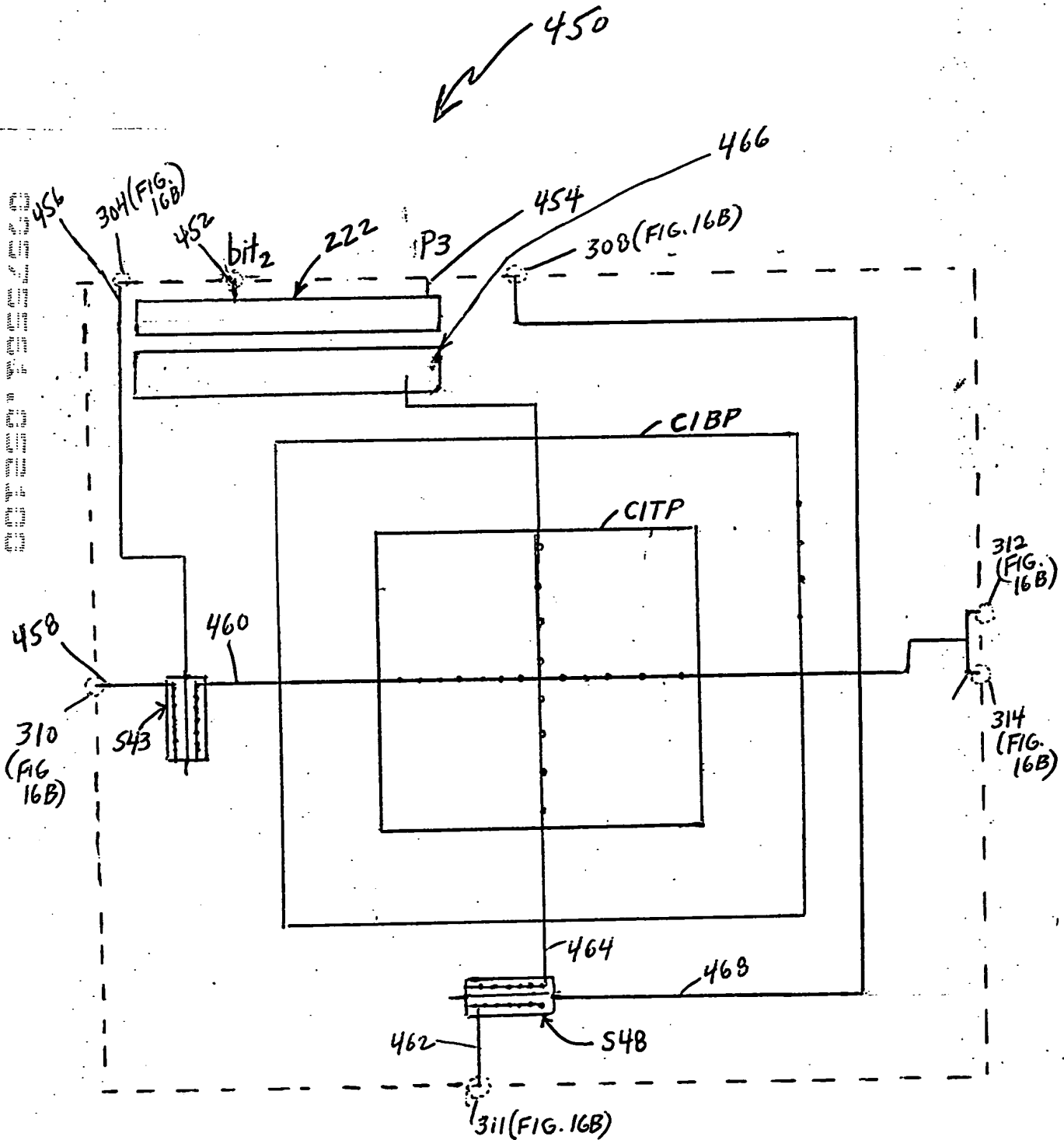


FIG 26

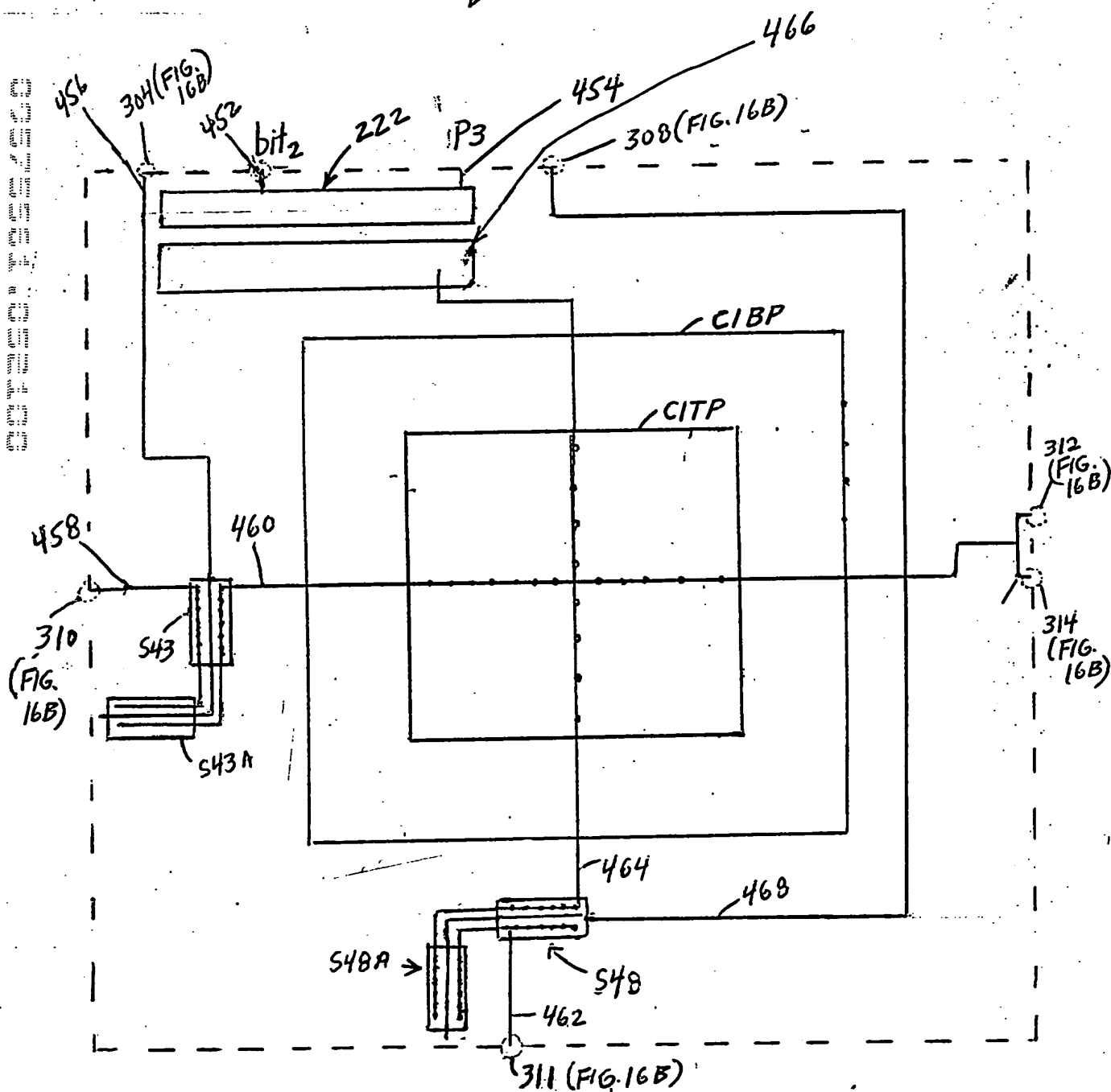


F1G 27

FIG 28A



450



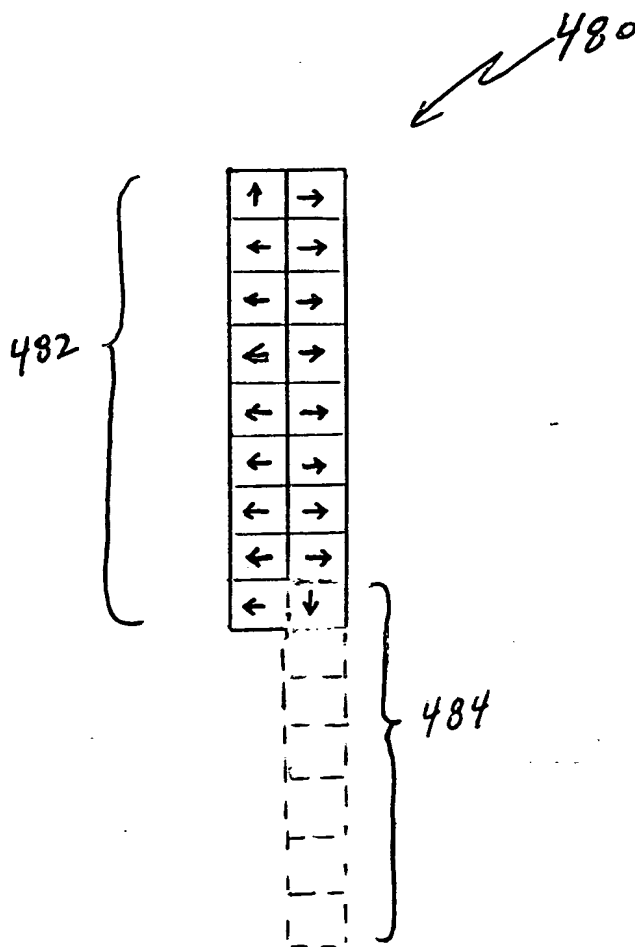


FIG. 29

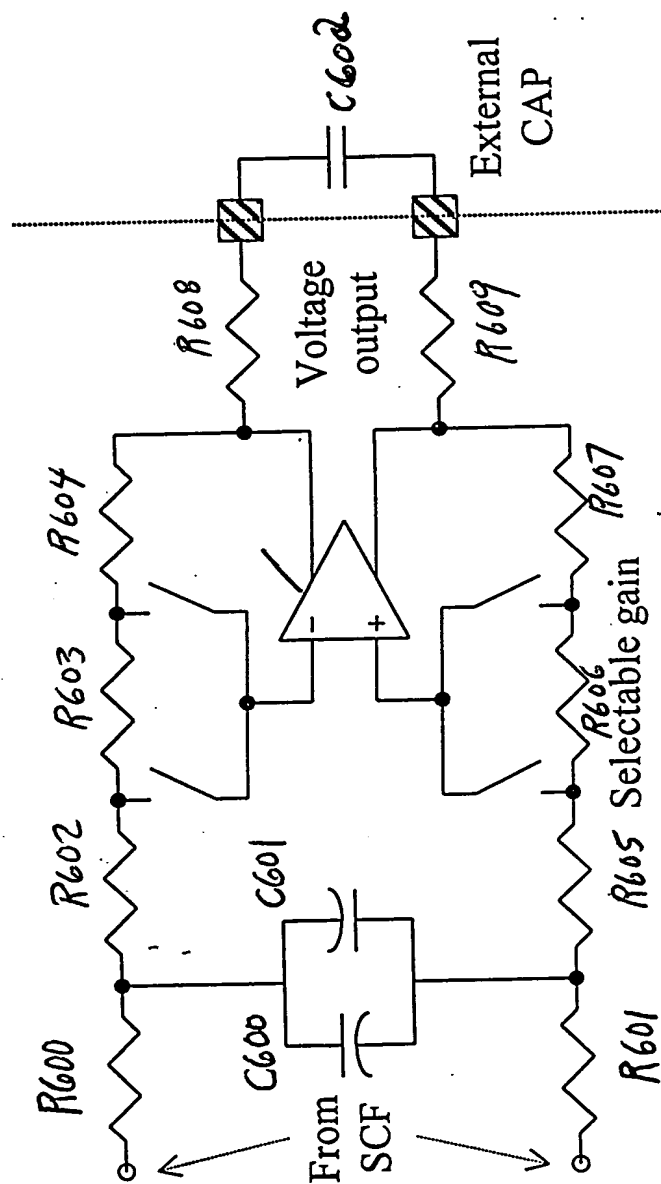


FIG. 30

150

500

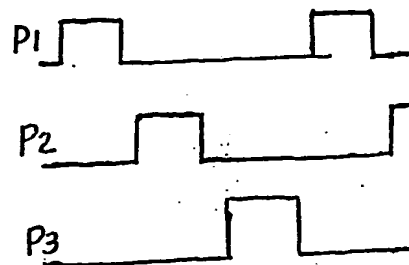
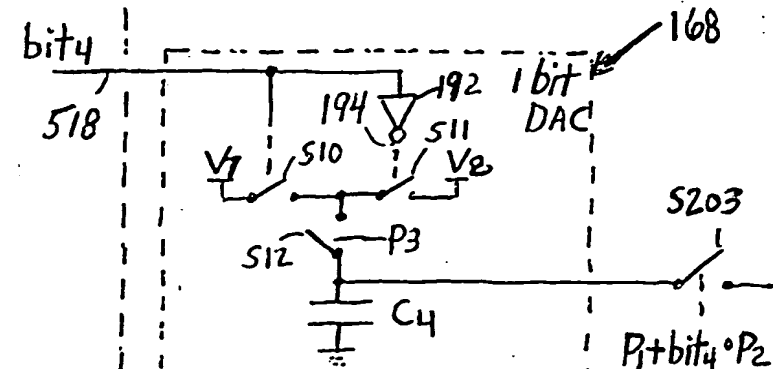
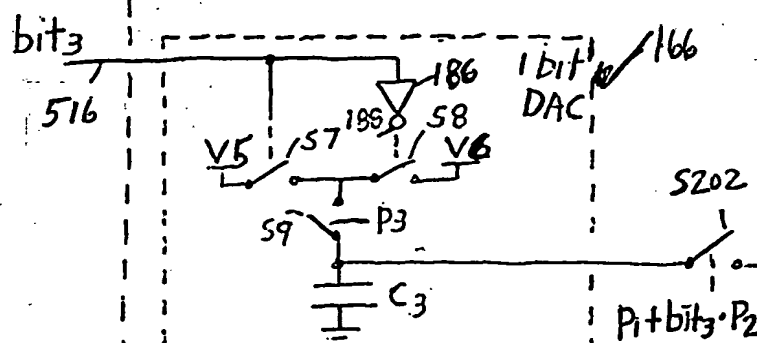
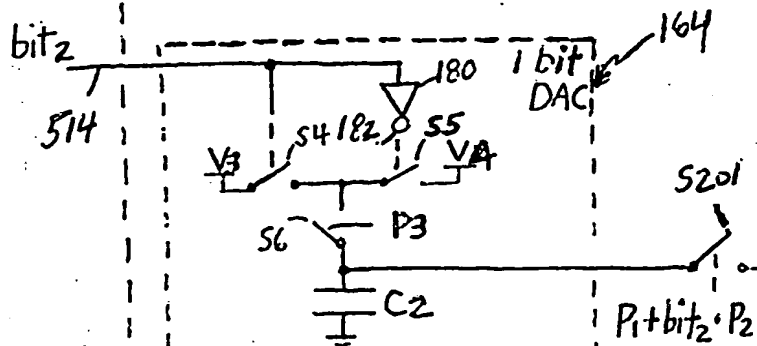
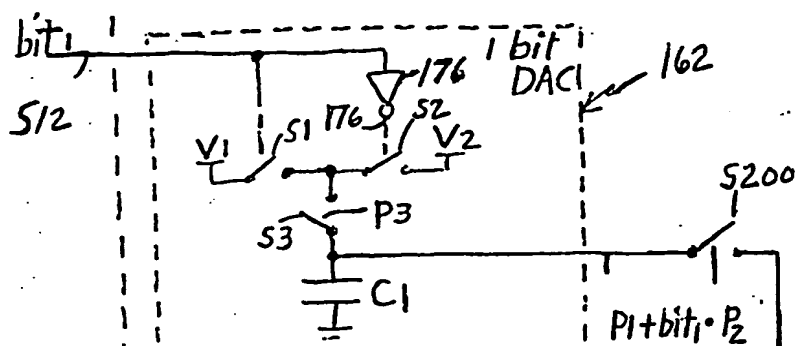


FIG.32

FIG.31

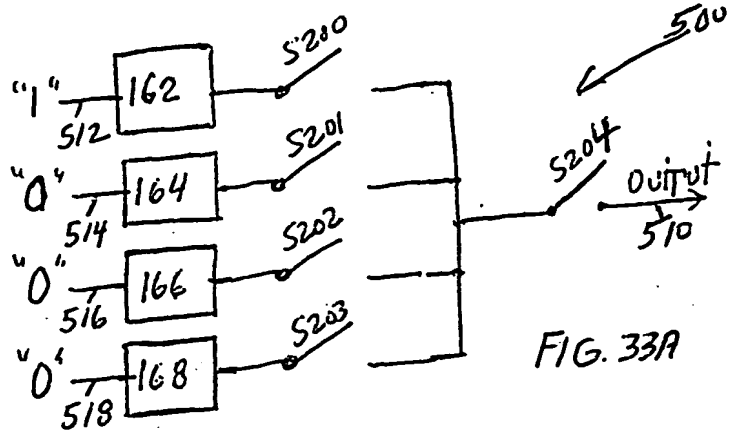


FIG. 33A

P1 "0"	$V(C_1) = V_{ref}$	$Q(C_1) = C \cdot V_{ref}$
P2 "0"	$V(C_2) = 0$	$Q(C_2) = 0$
P3 "1"	$V(C_3) = 0$	$Q(C_3) = 0$
	$V(C_4) = 0$	$Q(C_4) = 0$

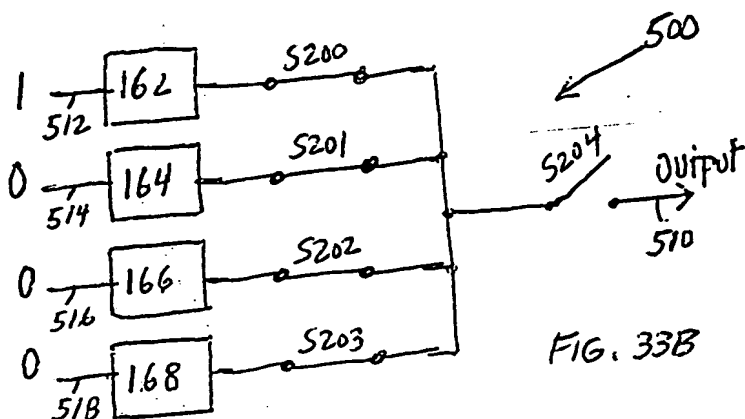


FIG. 33B

P1 "1"	$V(C_1) = V_{ref}/4$	$Q(C_1) = C \cdot V_{ref}/4$
P2 "0"	$V(C_2) = V_{ref}/4$	$Q(C_2) = C \cdot V_{ref}/4$
P3 "0"	$V(C_3) = V_{ref}/4$	$Q(C_3) = C \cdot V_{ref}/4$
	$V(C_4) = V_{ref}/4$	$Q(C_4) = C \cdot V_{ref}/4$

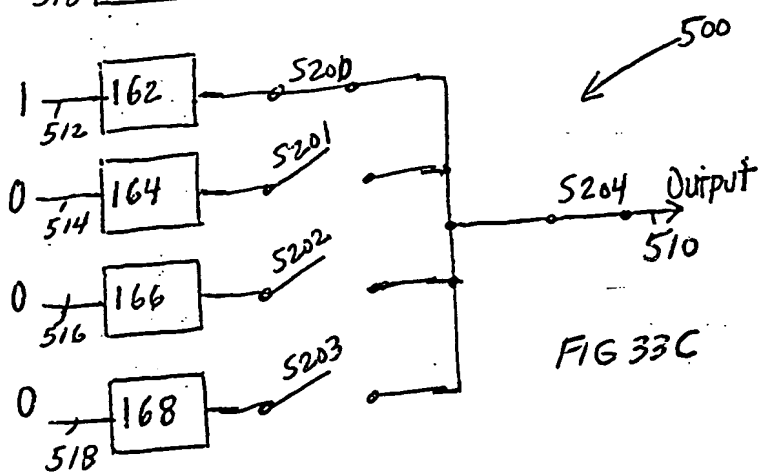
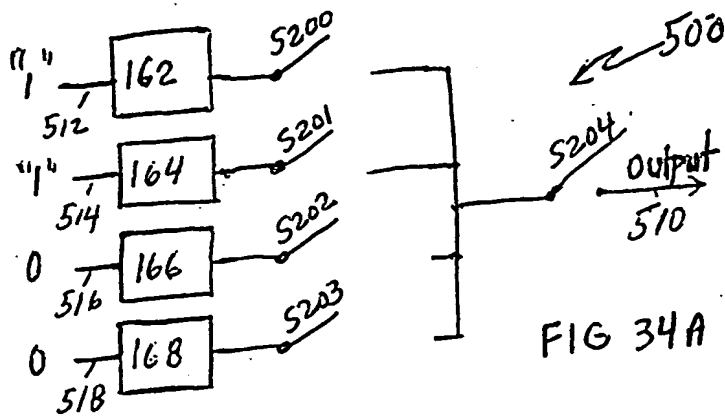


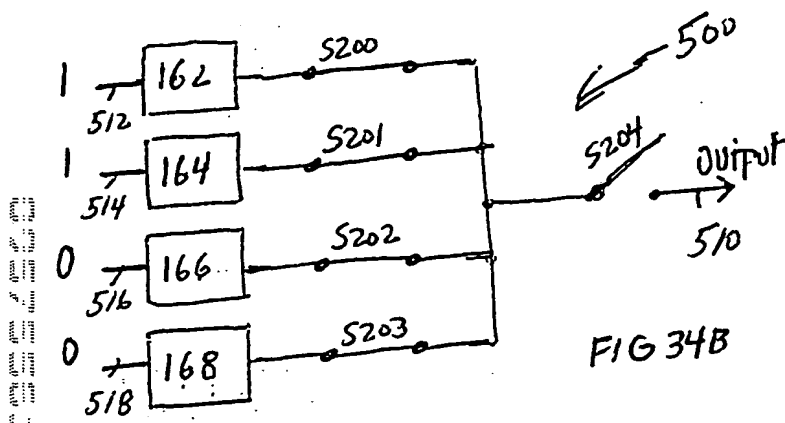
FIG. 33C

P1 "0"	$V(C_1) = V_{ref}/4$	$Q(C_1) = C \cdot V_{ref}/4$
P2 "1"	$V(C_2) = V_{ref}/4$	$Q(C_2) = C \cdot V_{ref}/4$
P3 "0"	$V(C_3) = V_{ref}/4$	$Q(C_3) = C \cdot V_{ref}/4$
	$V(C_4) = V_{ref}/4$	$Q(C_4) = C \cdot V_{ref}/4$

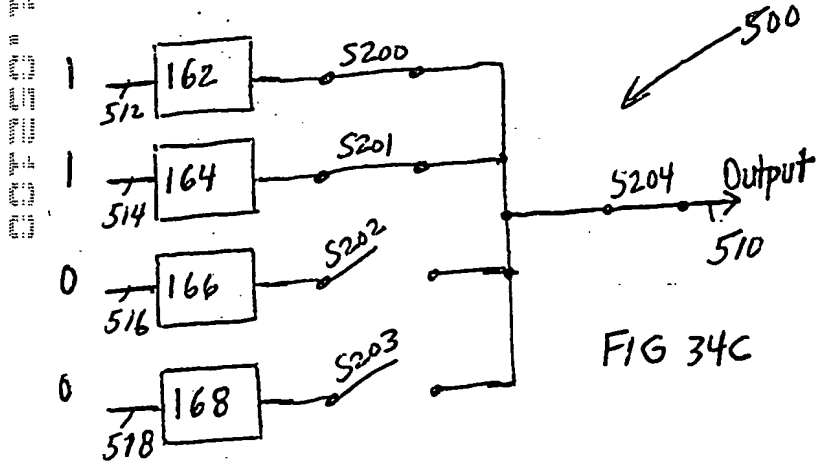
Q delivered to
output terminal
is $Q(C_1) = C \cdot V_{ref}/4$



P1 "0"	$V(C_1) = V_{ref}$	$Q(C_1) = C * V_{ref}$
P2 "0"	$V(C_2) = V_{ref}$	$Q(C_2) = C * V_{ref}$
P3 "1"	$V(C_3) = 0$	$Q(C_3) = 0$
	$V(C_4) = 0$	$Q(C_4) = 0$



P1 "1"	$V(C_1) = V_{ref}/2$	$Q(C_1) = C * V_{ref}/2$
P2 "0"	$V(C_2) = V_{ref}/2$	$Q(C_2) = C * V_{ref}/2$
P3 "0"	$V(C_3) = V_{ref}/2$	$Q(C_3) = C * V_{ref}/2$
	$V(C_4) = V_{ref}/2$	$Q(C_4) = C * V_{ref}/2$



P1 "0"	$V(C_1) = V_{ref}/2$	$Q(C_1) = C * V_{ref}/2$
P2 "1"	$V(C_2) = V_{ref}/2$	$Q(C_2) = C * V_{ref}/2$
P3 "0"	$V(C_3) = V_{ref}/2$	$Q(C_3) = C * V_{ref}/2$
	$V(C_4) = V_{ref}/2$	$Q(C_4) = C * V_{ref}/2$

Q delivered to output terminal
is $Q(C_1) + Q(C_2) =$

$$C * V_{ref}/2 + C * V_{ref}/2 = C * V_{ref}$$

800

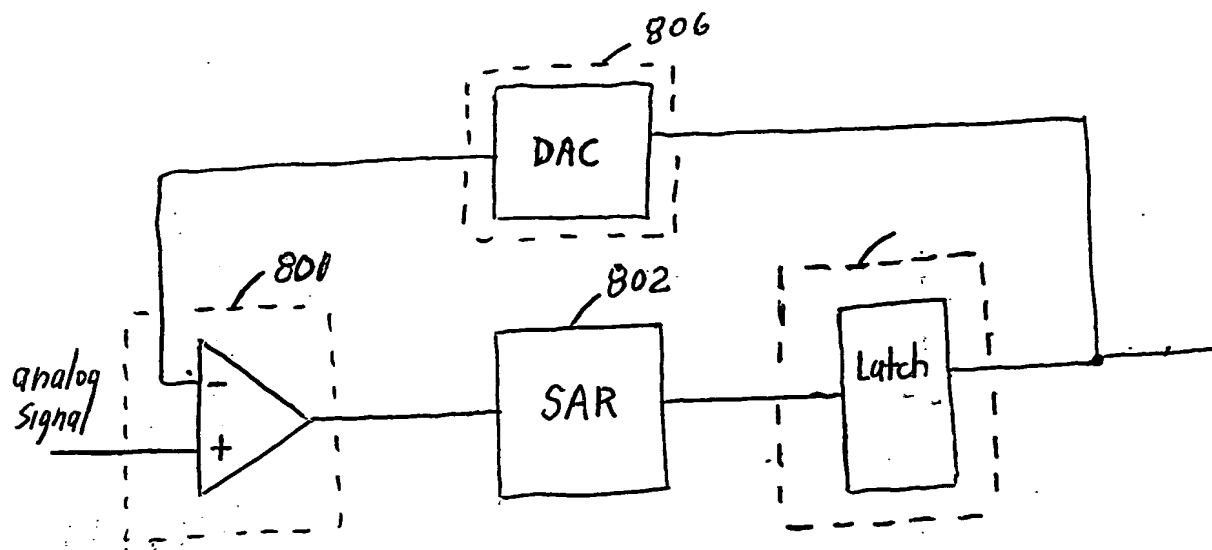


FIG. 35